

# L287B-SR

**Wi-Fi Dual-band 1X1 11a/b/g/n/ac +Bluetooth 5.0  
Combo Module Datasheet**



## L287B-SR Module Datasheet

**Office:** 6 Floor, Building U6, Junxiang U8 Park,  
Hangcheng Avenue, Bao'an District,  
Shenzhen City, CHINA

**Factory:** No.8, Litong Road, Liuyang Economic & Technical  
Development Zone, Changsha, Hunan, CHINA

**TEL:** +86-755-2955-8186

**Website:** www.fn-link.com

Customer Approval : \_\_\_\_\_ Company  
\_\_\_\_\_  
Title  
\_\_\_\_\_  
Signature  
\_\_\_\_\_  
Date  
\_\_\_\_\_  
Fn-Link

## Revision History

Version	Date	Revision Content	Draft	Approved
1.0	2021/03/23	Draft version	Lgp	Szs
1.1	2021/03/31	Correct typos	Wesley	Szs
1.2	2021/05/06	Pin map change	Wesley	Szs
1.3	2021/05/20	Change pin13 to NC	Wesley	Szs
1.4	2021/06/11	Refine section 1.3, 1.4, 2.1, 2.2, 4.2, 5.1, 6.1 and 7	Wesley	Qjp
1.5	2021/07/16	Add power consumption, refine section 2.1 and 3.1.	Wesley	Qjp
1.6	2021/08/18	Add notice for UART baud-rate and VCC power supply; correct typos.	Wesley	Qjp
1.7	2021/09/10	Change notice of UART baud-rate, add module photo, correct typos.	Wesley	Qjp

CONTENTS

**1 Overview..... 2**

    1.1 Introduction..... 2

    1.2 Features..... 2

    1.3 Block Diagram..... 2

    1.4 General Specification..... 3

    1.5 Recommended Operating Rating..... 3

    1.6 Power Consumption..... 3

**2 Wi-Fi RF Specification..... 4**

    2.1 2.4GHz RF Specification..... 4

    2.2 5GHz RF Specification..... 5

**3 Bluetooth Specification..... 7**

    3.1 Bluetooth Specification..... 7

**4 Pin Assignments..... 7**

    4.1 Pin Outline..... 8

    4.2 Pin Definition..... 8

**5 Dimensions..... 11**

    5.1 Module Picture..... 11

    5.2 Marking Description..... 11

    5.3 Module Physical Dimensions..... 12

    5.4 Layout Recommendation..... 13

**6 Power-up Sequence and Timing Specification..... 14**

    6.1 Power-up sequence..... 14

    6.2 SDIO Default Speed, High Speed Mode Timing..... 14

    6.3 SDIO SDR12, SDR25, SDR50 modes (up to 100 MHz) (1.8V)..... 15

    6.4 SDIO SDR104 mode (208 MHz) (1.8V)..... 16

    6.5 SDIO DDR50 mode (50 MHz) (1.8V)..... 17

    6.6 High-speed UART specifications..... 18

    6.7 Bluetooth PCM Timing..... 19

**7 Reference Design..... 21**

**8 Ordering Information..... 21**

**9 The Key Material List..... 22**

**10 Recommended Reflow Profile..... 22**

**11 Package Information..... 23**

    11.1 Reel..... 23

    11.2 Carrier Tape Detail..... 23

    11.3 Packaging Detail..... 24

    11.4 Moisture sensitivity..... 24

# 1 Overview

## 1.1 Introduction

L287B-SR has dual-band Wi-Fi and Bluetooth functionalities. It is based on NXP 88W8987 chipset, a highly-integrated IEEE 802.11a/b/g/n/ac MAC/Baseband/RF WLAN and Bluetooth Baseband/RF single chip.

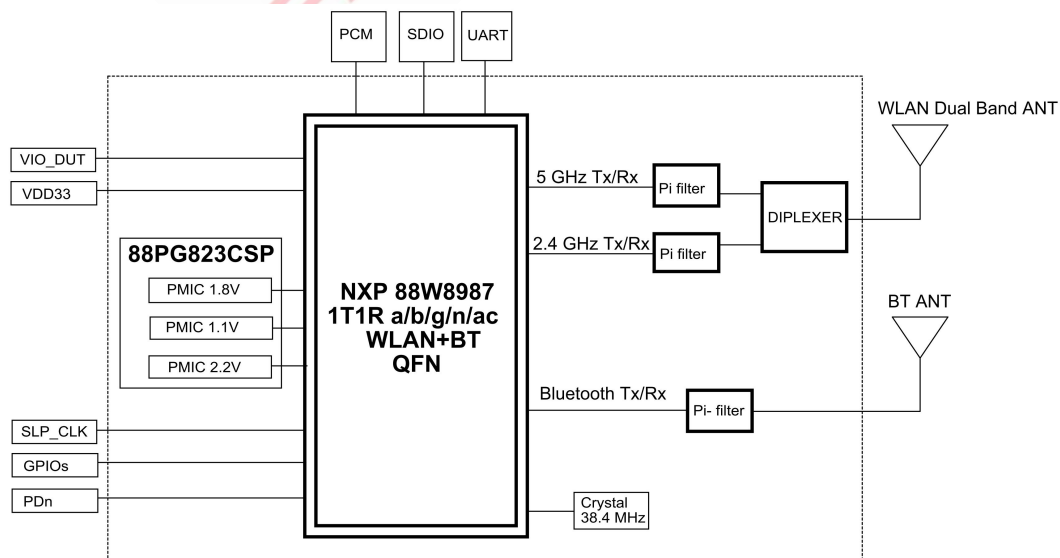
The module provides SDIO3.0 interface for Wi-Fi and HS-UART/PCM for Bluetooth.

L287B-SR can achieve up to a speed of 433.3Mbps with single stream 802.11ac WLAN connection. It is a perfect solution for a combination of Wi-Fi and BT technologies.

## 1.2 Features

- NXP 88W8987 inside
- CMOS MAC, Baseband PHY and RF in a single chip for IEEE 802.11 a/b/g/n/ac
- Support 802.11ac, 1x1 with data rates up to MCS9
- Maximum rate 433Mbps in 80MHz bandwidth
- SDIO3.0 interface for WLAN
- Support Bluetooth V5.0 features
- HS-UART and PCM interface for BT
- Bluetooth LE supports Broadcaster, Observer, Central, and Peripheral roles
- Supports link layer topology to be master and slave (connects up to 16 links)
- Wi-Fi/Bluetooth coexistence protocol support

## 1.3 Block Diagram



## 1.4 General Specification

Model Name	L287B-SR
Dimension	L x W x H: 15 x 13 x 2.15 mm (typical)
Wi-Fi Interface	SDIO3.0
BT Interface	UART / PCM
Operating temperature	-30°C to 85°C
Storage temperature	-40°C to 125°C

[Note] Baud-rate of UART interface is 115200 by default.

## 1.5 Recommended Operating Rating

	Min.	Typ.	Max.	Unit
Operating Temperature	-30	25	85	°C
VCC33	3.135	3.3	3.465	V
VDDIO	1.71	1.8	1.89	V

## 1.6 Power Consumption

[Note] The consumption is quite high while module initializing, please make sure the current supply of VCC33 power is greater than 1A.

Band	Mode		Current Consumption(Unit:mA) VCC33 = VIO = 3.3V
NA	Idle		57
2.4GHz	Continue Tx	11b 1Mbps @17dBm	483
		11g 6Mbps @17dBm	457
		11n HT20 mcs0@14dBm	475
		11n HT40 mcs0@14dBm	464
	Continue Rx	11b 1Mbps	72
		11n HT40 mcs7	72
5GHz	Continue Tx	11a 6Mbps @17.5dBm	470
		11ac VHT20 mcs0 @17dBm	492
		11ac VHT40 mcs0 @17dBm	485
		11ac VHT80 mcs0 @11dBm	292
	Continue Rx	11a 6Mbps	70
		11n HT40 mcs7	82
		11ac VHT20 mcs9	70
		11ac VHT80 mcs9	93

## 2 Wi-Fi RF Specification

### 2.1 2.4GHz RF Specification

Feature	Description			
WLAN Standard	IEEE 802.11 b/g/n Wi-Fi compliant			
Frequency Range	2.400 GHz ~ 2.4835 GHz (2.4 GHz ISM Band)			
Number of Channels	2.4GHz: Ch1 ~ Ch14			
Spectrum Mask	Min. b/g/n	Typ. b/g/n	Max. b/g/n	Unit b/g/n
1st side lobes(to fc ± 11MHZ)	-	-43/-30/-40	-	dBr
2st side lobes(to fc ± 22MHZ)	-	-52/-33/-58	-	dBr
Freq. Tolerance	-20/-20/-20	-	20/20/20	ppm
Test Items	Typical Value			EVM
Output Power	802.11b /11Mbps: 17dBm ± 1.5 dB			EVM ≤ -9dB
	802.11g /54Mbps: 15dBm ± 1.5 dB			EVM ≤ -25dB
	802.11n /MCS7: 14dBm ± 1.5 dB			EVM ≤ -28dB
Test Items	TYP Test Value			Standard Value
SISO Receive Sensitivity (11b,20MHz) @8% PER	- 1Mbps	≤ -92 dBm		≤ -85 dBm
	- 11Mbps	≤ -82 dBm		≤ -76 dBm
SISO Receive Sensitivity (11g,20MHz) @10% PER	- 6Mbps	≤ -86 dBm		≤ -82 dBm
	- 54Mbps	≤ -71 dBm		≤ -65 dBm
SISO Receive Sensitivity (11n,20MHz) @10% PER	- MCS=0	≤ -86 dBm		≤ -82 dBm
	- MCS=7	≤ -67 dBm		≤ -64 dBm
SISO Receive Sensitivity (11n ,40MHz) @10% PER	- MCS=0	≤ -83 dBm		≤ -79 dBm
	- MCS=7	≤ -65 dBm		≤ -61 dBm
Maximum Input Level	802.11b: -10 dBm			
	802.11g/n: -20 dBm			
Antenna Reference	Small antennas with 0~2 dBi peak gain			

## 2.2 5GHz RF Specification

Feature	Description	
WLAN Standard	IEEE 802.11a/n/ac 1x1, Wi-Fi compliant	
Frequency Range	5.150 GHz ~ 5.850 GHz (5.0 GHz Band)	
Number of Channels	5.0GHz: Please see the table <sup>1</sup>	
Test Items	Typical Value	EVM
Output Power	802.11a /54Mbps: 15 dBm ± 1.5 dB	EVM ≤ -25dB
	802.11n /MCS7: 14 dBm ± 1.5 dB	EVM ≤ -28dB
	802.11ac	EVM ≤ -32dB
	VHT20/MCS8: 13 dBm ± 1.5 dB	
VHT40/MCS9: 13 dBm ± 1.5 dB		
VHT80/MCS9: 11 dBm ± 1.5 dB		
Test Items	Test Value	Standard Value
Receive Sensitivity (11a, 20MHz) @10% PER	- 6Mbps ≤ -86 dBm	≤ -82 dBm
	- 54Mbps ≤ -71 dBm	≤ -65 dBm
Receive Sensitivity (11n,20MHz) @10% PER	- MCS=0 ≤ -86 dBm	≤ -82 dBm
	- MCS=7 ≤ -67 dBm	≤ -64 dBm
Receive Sensitivity (11n,40MHz) @10% PER	- MCS=0 ≤ -82 dBm	≤ -79 dBm
	- MCS=7 ≤ -64 dBm	≤ -61 dBm
Receive Sensitivity (11ac,20MHz) @10% PER	- MCS=0 ≤ -85 dBm	≤ -82 dBm
	- MCS=8 ≤ -64 dBm	≤ -59 dBm
Receive Sensitivity (11ac,40MHz) @10% PER	- MCS=0 ≤ -82 dBm	≤ -79 dBm
	- MCS=9 ≤ -59 dBm	≤ -54 dBm
Receive Sensitivity (11ac,80MHz) @10% PER	- MCS=0 ≤ -79 dBm	≤ -76 dBm
	- MCS=9 ≤ -55 dBm	≤ -51 dBm
Maximum Input Level	802.11a/n: -30 dBm	
Antenna Reference	Small antennas with 0~2 dBi peak gain	

Conditions : VCC=3.3V ; VDDIO=1.8V ; Temp:25°C

### <sup>1</sup>5GHz(20MHz) Channel table

Band range	Operating Channel Numbers	Channel center frequencies (MHz)
5180MHz~5240MHz	36	5180
	40	5200
	44	5220
	48	5240
5260MHz~5320MHz	52	5260



	56	5280
	60	5300
	64	5320
5550MHz~5700MHz	100	5500
	104	5520
	108	5540
	112	5560
	116	5580
	120	5600
	124	5620
	128	5640
	132	5660
	136	5680
	140	5700
5745MHz~5825MHz	149	5745
	153	5765
	157	5785
	161	5805
	165	5825

## 3 Bluetooth Specification

### 3.1 Bluetooth Specification

Feature	Description		
<b>General Specification</b>			
Bluetooth Standard	Bluetooth V5.0		
Host Interface	UART		
Antenna Reference	Small antennas with 0~2 dBi peak gain		
Frequency Band	2402 MHz ~ 2480 MHz		
Number of Channels	79 channels		
Modulation	GFSK, $\pi/4$ -DQPSK, 8DPSK		
<b>RF Specification</b>			
	<b>Min.</b>	<b>Typical.</b>	<b>Max.</b>
Output Power (BR/LE)		10 dBm	
Output Power (EDR) <sup>Note1</sup>		7 dBm	
Sensitivity @ BER=0.1% for GFSK (1Mbps) <sup>Note2</sup>		-92dBm	
Sensitivity @ BER=0.01% for $\pi/4$ -DQPSK (2Mbps) <sup>Note2</sup>		-86dBm	
Sensitivity @ BER=0.01% for 8DPSK (3Mbps) <sup>Note2</sup>		-85dBm	
Maximum Input Level	GFSK (1Mbps): -20dBm		
	$\pi/4$ -DQPSK (2Mbps): -20dBm		
	8DPSK (3Mbps): -20dBm		

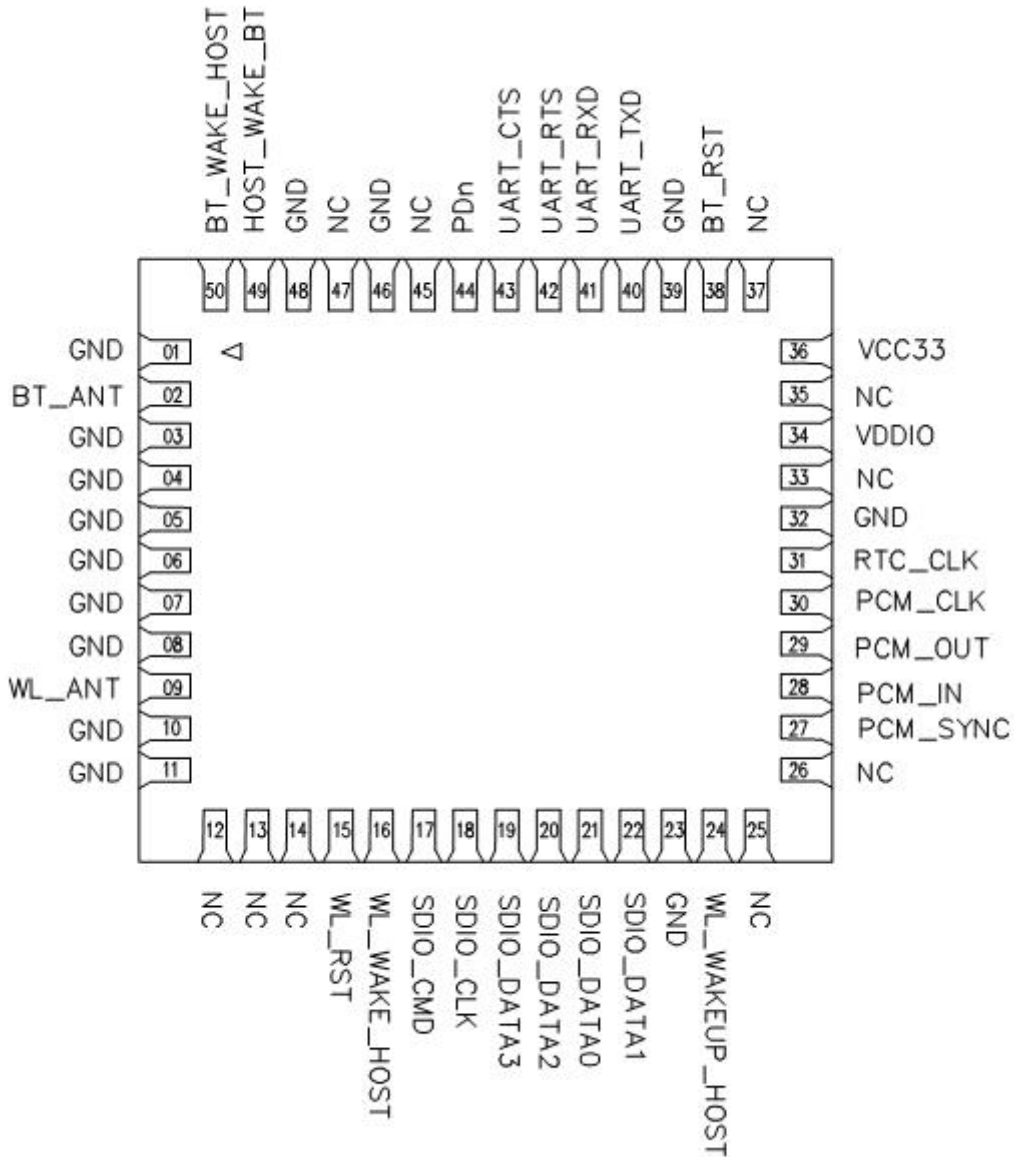
Note1: By default, 88W8987's EDR TX power is 3dBm less than BR TX power.

Note2: Desense of ~7 dB at CH 2419 MHz, ~4 dB at CH 2432 MHz, ~3 dB at 2457 MHz, ~4 dB at 2458 MHz due to internal clock harmonics of chipset.

## 4 Pin Assignments

### 4.1 Pin Outline

< TOP VIEW >



### 4.2 Pin Definition

NO	Name	Type	Description	Voltage
1	GND	—	Ground connections	
2	BT_ANT	I/O	RF I/O port for BT	
3	GND	—	Ground connections	

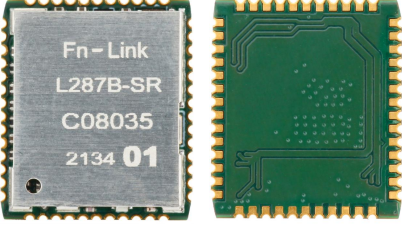
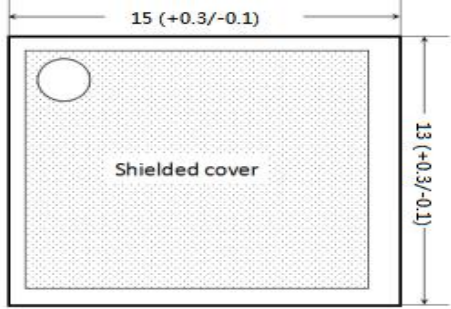
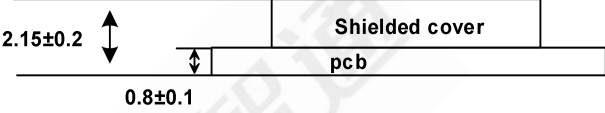
4	GND	—	Ground connections	
5	GND	—	Ground connections	
6	GND	—	Ground connections	
7	GND	—	Ground connections	
8	GND	—	Ground connections	
9	WL_ANT	I/O	RF I/O port for dual band Wi-Fi	
10	GND	—	Ground connections	
11	GND	—	Ground connections	
12	NC	—	No connect	
13	NC	—	No connect	
14	NC	—	No connect	
15	WL_RST	I	WLAN independent reset, internal pull up	1.8V
16	WL_WAKE_HOST	O	WLAN wake-up HOST, internal pull up	1.8V
17	SDIO_CMD	I/O	SDIO command line	1.8V
18	SDIO_CLK	I/O	SDIO clock line	1.8V
19	SDIO_DATA_3	I/O	SDIO data line 3	1.8V
20	SDIO_DATA_2	I/O	SDIO data line 2	1.8V
21	SDIO_DATA_0	I/O	SDIO data line 0	1.8V
22	SDIO_DATA_1	I/O	SDIO data line 1	1.8V
23	GND	—	Ground connections	
24	WL_WAKE_HOST	O	WLAN wake-up HOST, Internally short to module PIN 16	1.8V
25	NC	—	No connect	
26	NC	—	No connect	
27	PCM_SYNC	I/O	PCM sync signal	1.8V
28	PCM_IN	I	PCM data input	1.8V
29	PCM_OUT	O	PCM Data output	1.8V
30	PCM_CLK	I/O	PCM clock	1.8V
31	RTC_CLK	I	External Low Power Clock input (32.768KHz) If not used keep NC	VDDIO
32	GND	—	Ground connections	
33	NC	—	No connect	
34	VDDIO	P	I/O Voltage supply input	1.8V

35	NC	—	No connect	
36	VCC33	P	Main power voltage source input	3.3V
37	NC	—	No connect	
38	BT_RST	I	Bluetooth independent reset, internal pull up	1.8V
39	GND	—	Ground connections	
40	UART_TXD	O	Bluetooth UART interface	1.8V
41	UART_RXD	I	Bluetooth UART interface	1.8V
42	UART_RTS_N	O	Bluetooth UART interface	1.8V
43	UART_CTS_N	I	Bluetooth UART interface	1.8V
44	PDn	I	Full Power-down, active low internal pull up	1.8V to 3.3V
45	NC	—	No connect	
46	GND	—	Ground connections	
47	NC	—	No connect	
48	GND	—	Ground connections	
49	HOST_WAKE_BT	I	HOST wake-up Bluetooth device, internal pull up	1.8V
50	BT_WAKE_HOST	O	Bluetooth device to wake-up HOST, internal pull up	1.8V

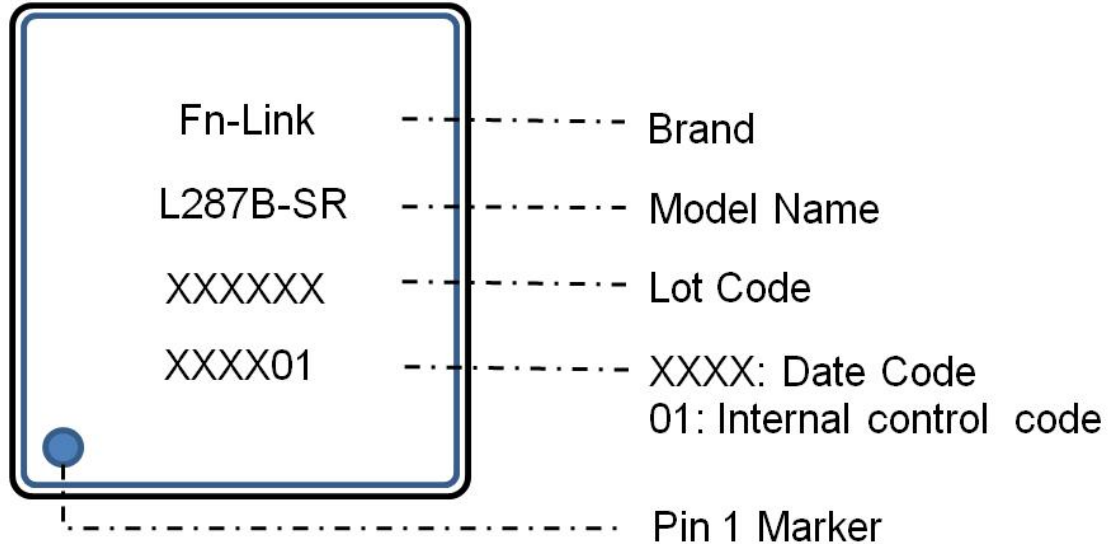
P:POWER I:INPUT O:OUTPUT VDDIO:1.8V

## 5 Dimensions

### 5.1 Module Picture

<p>L x W : 15 x 13 (+0.3/-0.1) mm</p> 	
<p>H: 2.15 (±0.2) mm</p>	
<p>Weight</p>	<p>0.855g</p>

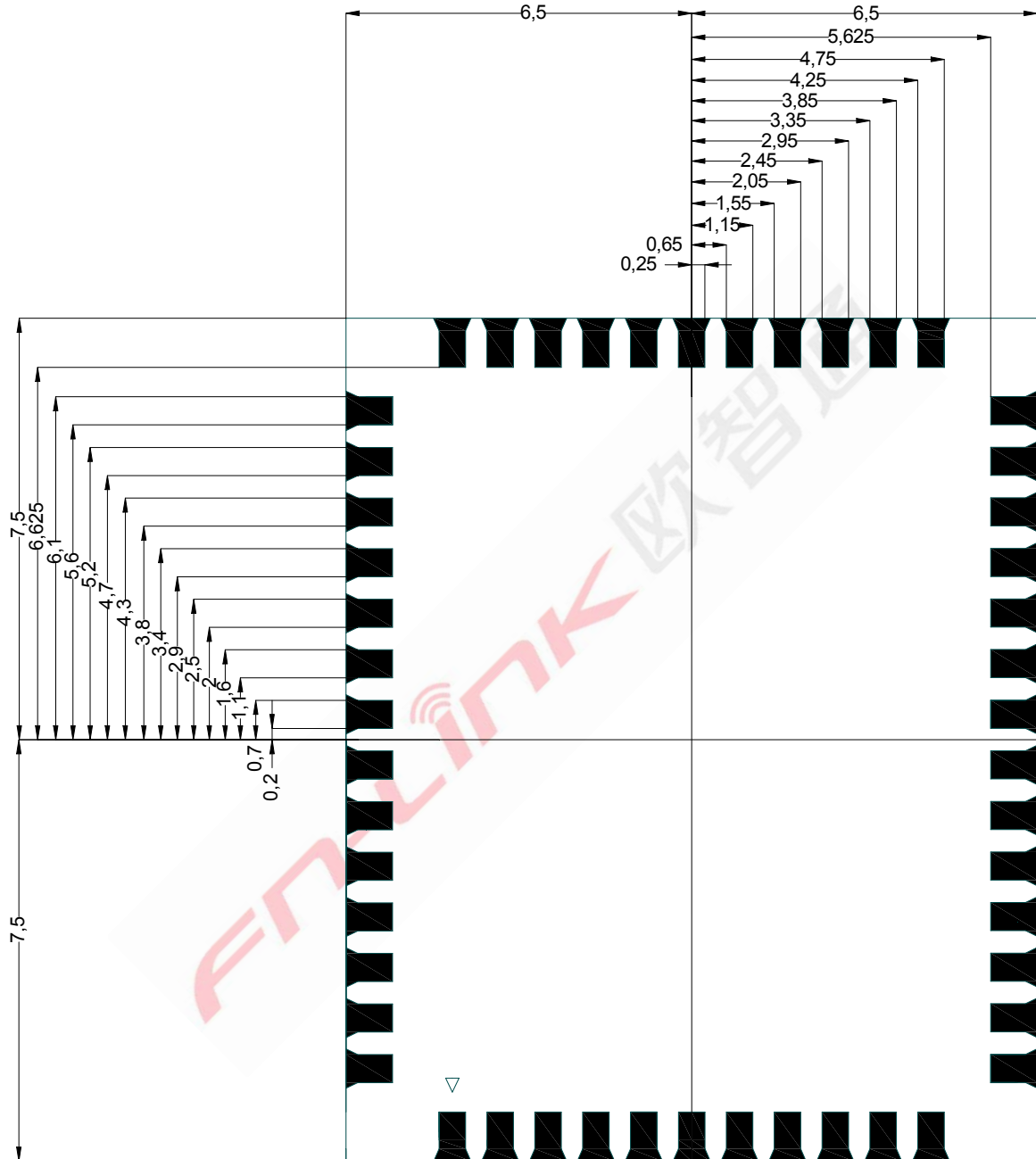
### 5.2 Marking Description



### 5.3 Module Physical Dimensions

(Unit: mm)

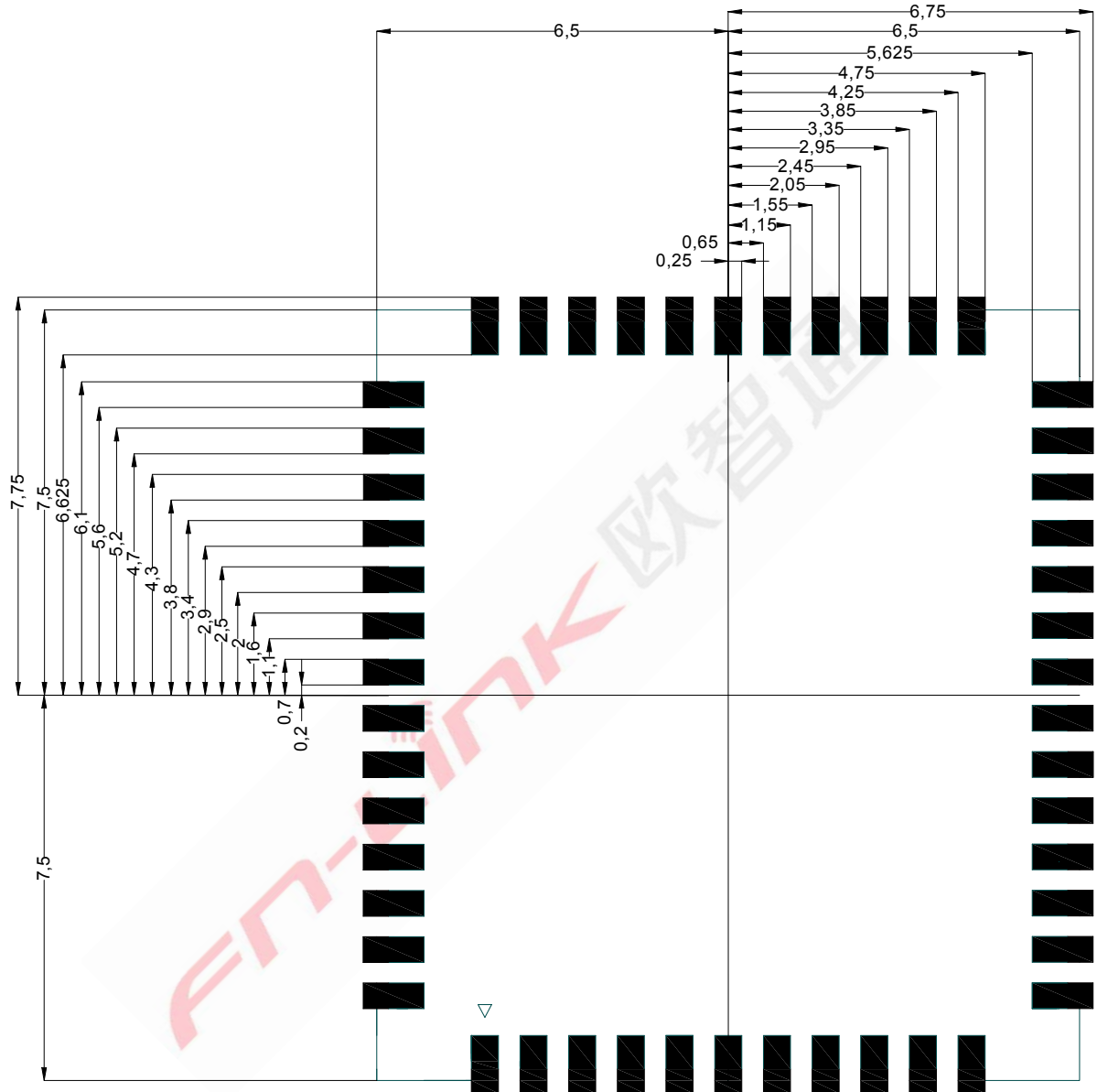
< TOP VIEW >



### 5.4 Layout Recommendation

(Unit: mm)

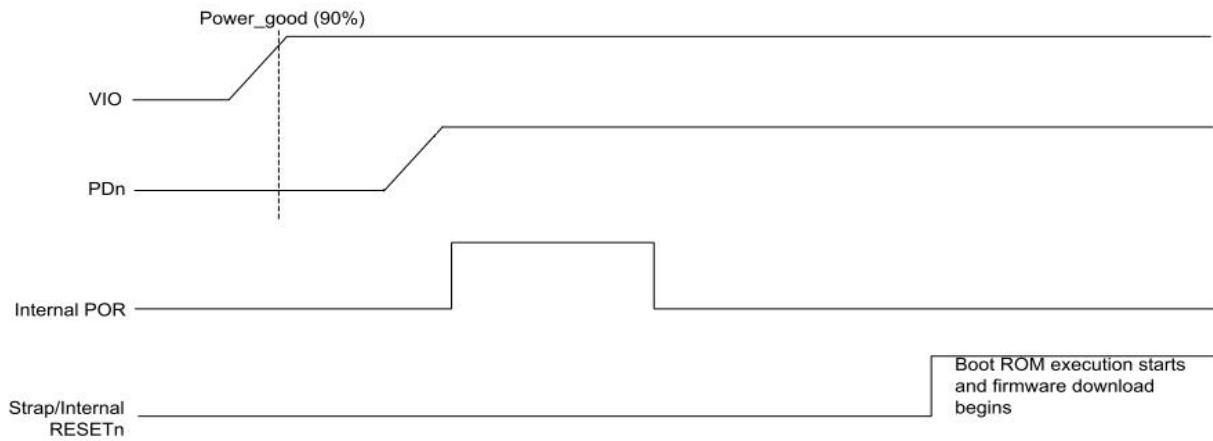
< TOP VIEW >





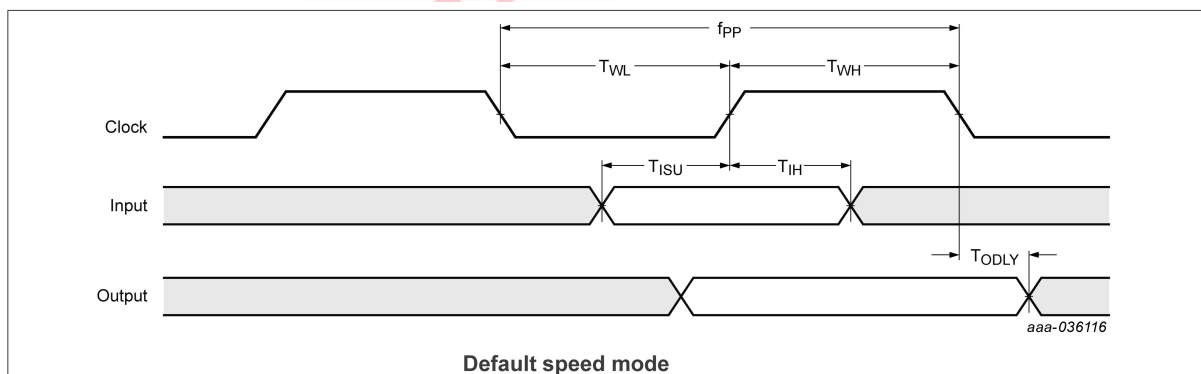
## 6 Power-up Sequence and Timing Specification

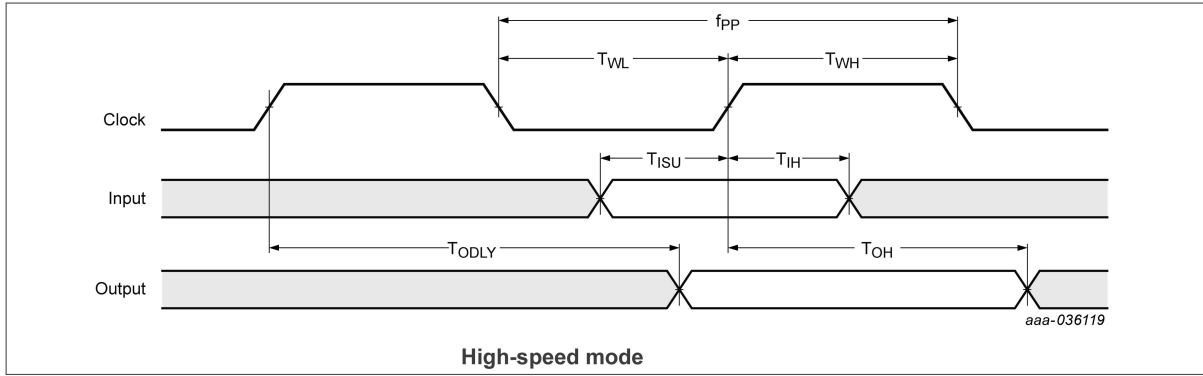
### 6.1 Power-up sequence



- VDDIO must be good (90%) before or at the same time VCC33 starts ramping up.
- VDDIO must be good (90%) before or at the same time PDn starts ramping up.
- Ramp-up time of VDDIO must be <100 ms.
- All supplies must be monotonic.

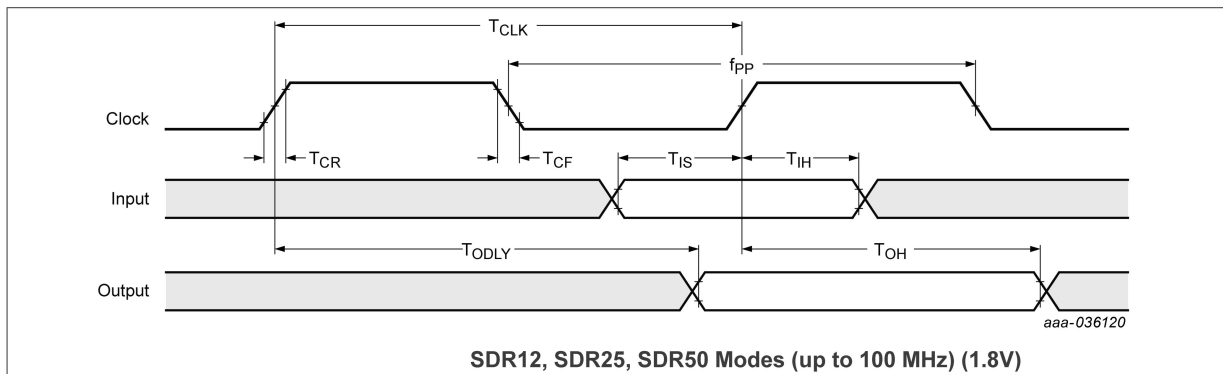
### 6.2 SDIO Default Speed, High Speed Mode Timing





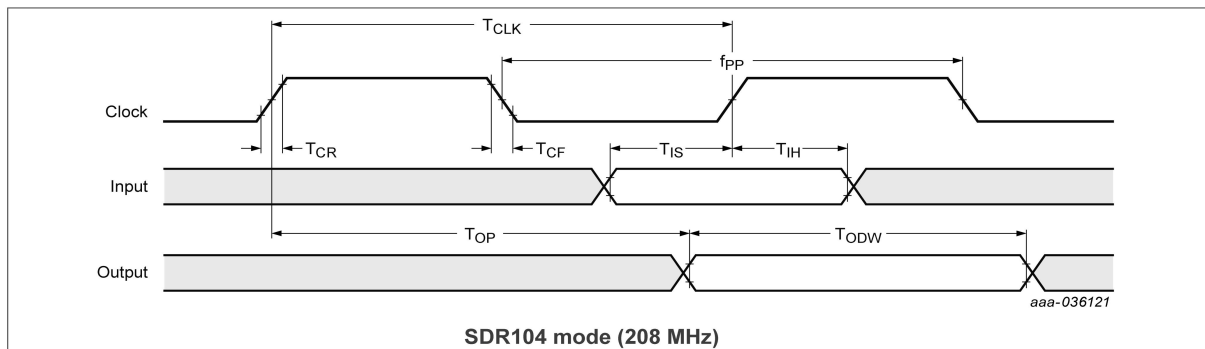
Symbol	Parameter	Condition	Min	Typ	Max	Unit
$f_{PP}$	Clock frequency	Normal	0	--	25	MHz
		High-speed	0	--	50	MHz
$T_{WL}$	Clock low time	Normal	10	--	--	ns
		High-speed	7	--	--	ns
$T_{WH}$	Clock high time	Normal	10	--	--	ns
		High-speed	7	--	--	ns
$T_{ISU}$	Input setup time	Normal	5	--	--	ns
		High-speed	6	--	--	ns
$T_{IH}$	Input hold time	Normal	5	--	--	ns
		High-speed	2	--	--	ns
$T_{ODLY}$	Output delay time	Normal	--	--	14	ns
	CL ≤ 40 pF (1 card)	High-speed	--	--	14	ns
$T_{OH}$	Output hold time	High-speed	2.5	--	--	ns

### 6.3 SDIO SDR12, SDR25, SDR50 modes (up to 100 MHz) (1.8V)



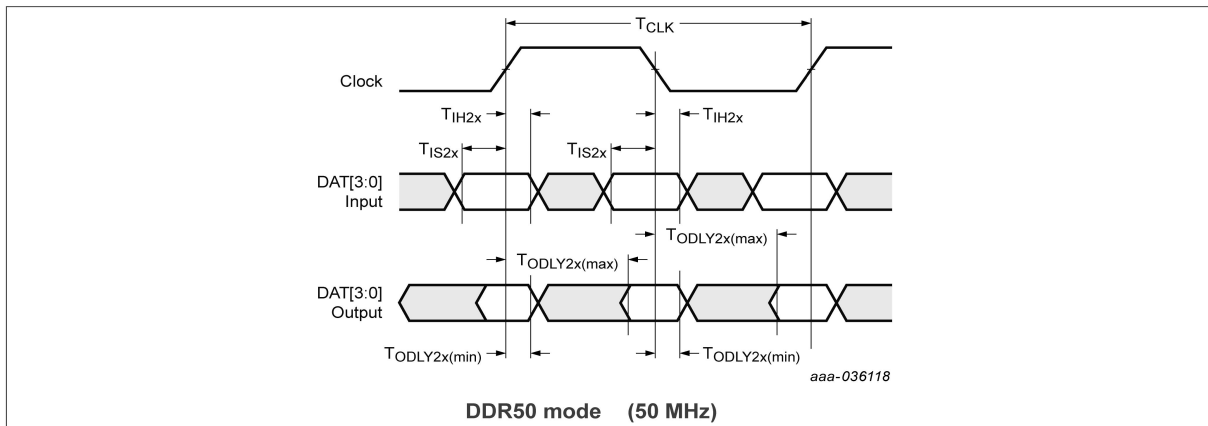
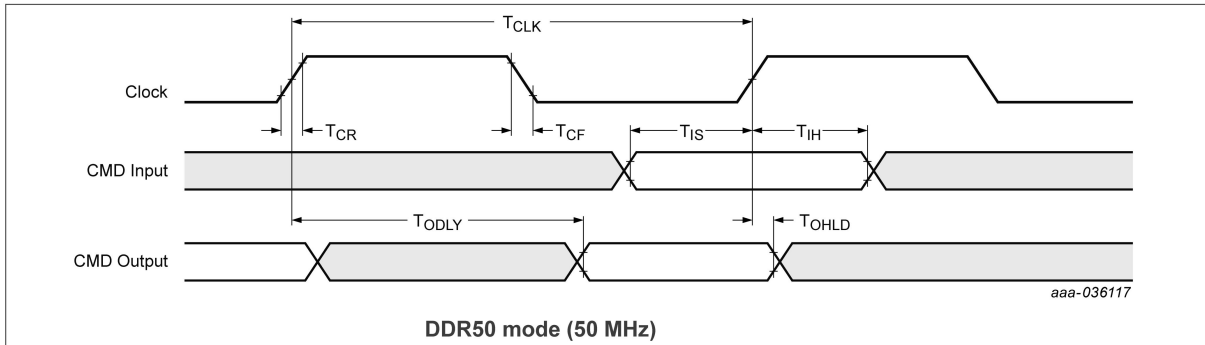
Symbol	Parameter	Condition	Min	Typ	Max	Units
f <sub>PP</sub>	Clock frequency	SDR12/25/50	25	--	100	MHz
T <sub>IS</sub>	Input setup time	SDR12/25/50	3	--	--	ns
T <sub>IH</sub>	Input hold time	SDR12/25/50	0.8	--	--	ns
T <sub>CLK</sub>	Clock time	SDR12/25/50	10	--	40	ns
T <sub>CR</sub> , T <sub>CF</sub>	Rise time, fall time T <sub>CR</sub> , T <sub>CF</sub> < 2 ns (max) at 100 MHz C <sub>CARD</sub> = 10 pF	SDR12/25/50	--	--	0.2*T <sub>CLK</sub>	ns
T <sub>ODLY</sub>	Output delay time C <sub>L</sub> ≤ 30 pF	SDR12/25/50	--	--	7.5	ns
T <sub>OH</sub>	Output hold time C <sub>L</sub> = 15 pF	SDR12/25/50	1.5	--	--	ns

### 6.4 SDIO SDR104 mode (208 MHz) (1.8V)



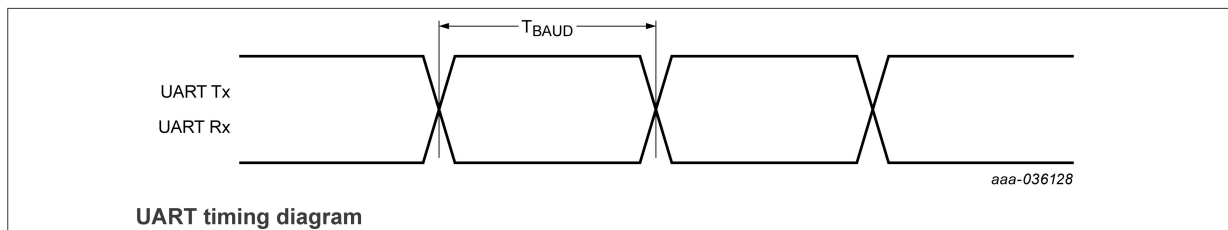
Symbol	Parameter	Condition	Min	Typ	Max	Unit
f <sub>PP</sub>	Clock frequency	SDR104	0	--	208	MHz
T <sub>IS</sub>	Input setup time	SDR104	1.4	--	--	ns
T <sub>IH</sub>	Input hold time	SDR104	0.8	--	--	ns
T <sub>CLK</sub>	Clock time	SDR104	4.8	--	--	ns
T <sub>CR</sub> , T <sub>CF</sub>	Rise time, fall time T <sub>CR</sub> , T <sub>CF</sub> < 0.96 ns (max) at 208 MHz C <sub>CARD</sub> = 10 pF	SDR104	--	--	0.2*T <sub>CLK</sub>	ns
T <sub>OP</sub>	Card output phase	SDR104	0	--	10	ns
T <sub>ODW</sub>	Output timing of variable data window	SDR104	2.88	--	--	ns

### 6.5 SDIO DDR50 mode (50 MHz) (1.8V)



Symbol	Parameter	Condition	Min	Typ	Max	Units
<b>Clock</b>						
T <sub>CLK</sub>	Clock time 50 MHz (max) between rising edges	DDR50	20	--	--	ns
T <sub>CR</sub> , T <sub>CF</sub>	Rise time, fall time T <sub>CR</sub> , T <sub>CF</sub> < 4.00 ns (max) at 50 MHz C <sub>CARD</sub> = 10 pF	DDR50	--	--	0.2*T <sub>CLK</sub>	ns
Clock Duty	--	DDR50	45	--	55	%
<b>CMD Input (referenced to clock rising edge)</b>						
T <sub>IS</sub>	Input setup time C <sub>CARD</sub> ≤ 10 pF (1 card)	DDR50	6	--	--	ns
T <sub>IH</sub>	Input hold time C <sub>CARD</sub> ≤ 10 pF (1 card)	DDR50	0.8	--	--	ns
<b>CMD Output (referenced to clock rising edge)</b>						
T <sub>ODLY</sub>	Output delay time during data transfer mode C <sub>L</sub> ≤ 30 pF (1 card)	DDR50	--	--	13.7	ns
T <sub>OHLd</sub>	Output hold time C <sub>L</sub> ≥ 15 pF (1 card)	DDR50	1.5	--	--	ns
<b>DAT[3:0] Input (referenced to clock rising and falling edges)</b>						
T <sub>IS2x</sub>	Input setup time C <sub>CARD</sub> ≤ 10 pF (1 card)	DDR50	3	--	--	ns
T <sub>IH2x</sub>	Input hold time C <sub>CARD</sub> ≤ 10 pF (1 card)	DDR50	0.8	--	--	ns
<b>DAT[3:0] Output (referenced to clock rising and falling edges)</b>						
T <sub>ODLY2x (max)</sub>	Output delay time during data transfer mode C <sub>L</sub> ≤ 25 pF (1 card)	DDR50	--	--	7.0	ns
T <sub>ODLY2x (min)</sub>	Output hold time C <sub>L</sub> ≥ 15 pF (1 card)	DDR50	1.5	--	--	ns

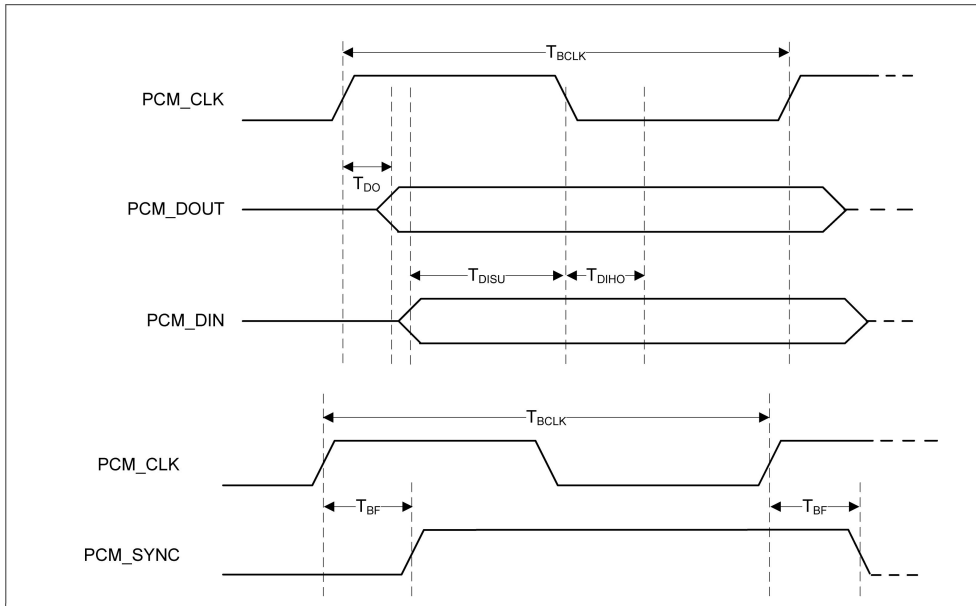
## 6.6 High-speed UART specifications



Symbol	Parameter	Condition	Min	Typ	Max	Unit
T <sub>BAUD</sub>	Baud rate	38.4 MHz input clock	250	--	--	ns

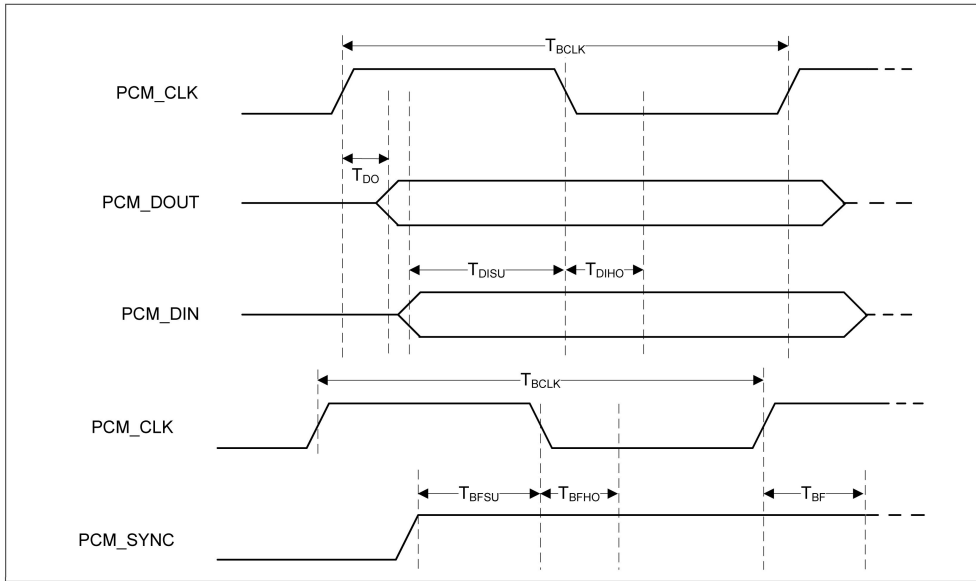
## 6.7 Bluetooth PCM Timing

### Master Mode



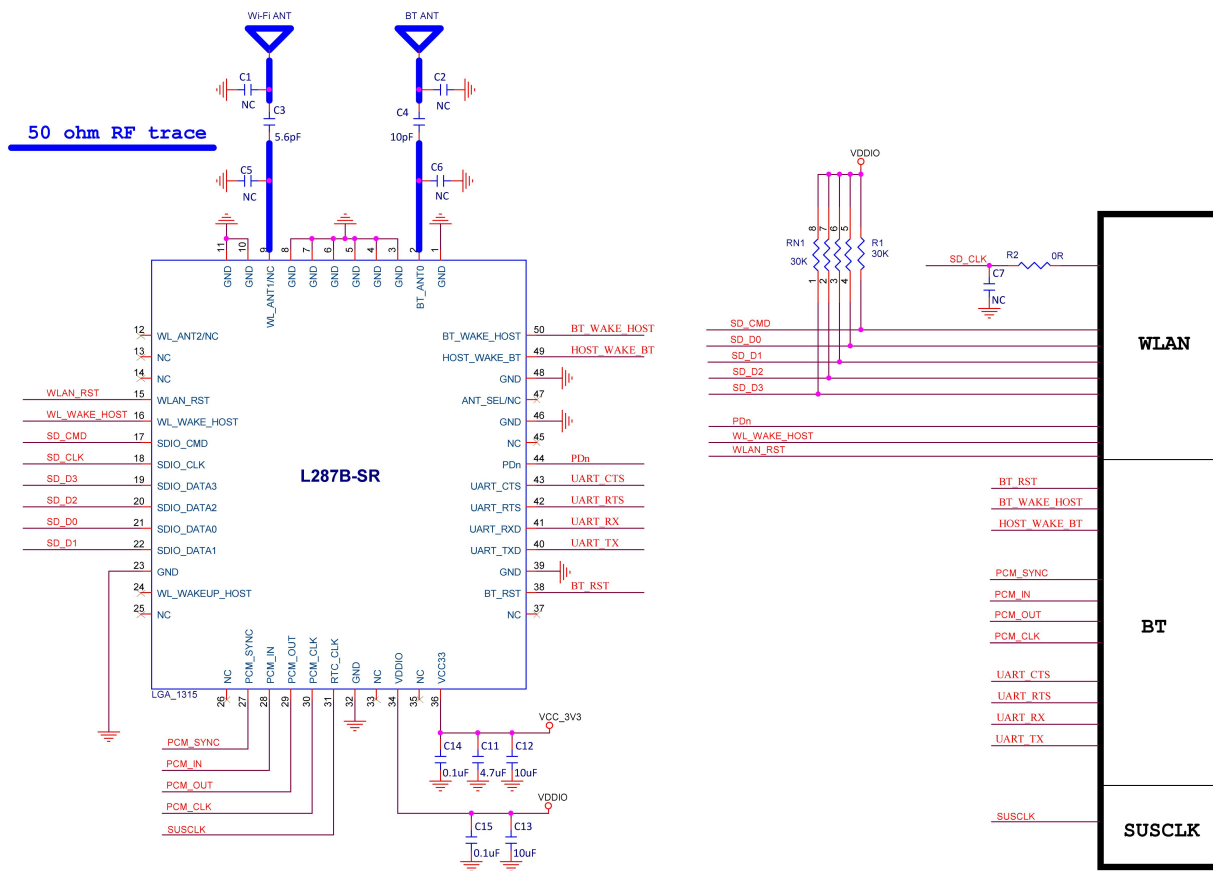
Symbol	Parameter	Condition	Min	Typ	Max	Unit
$F_{BCLK}$	Bit clock frequency	--	--	2/2.048	--	MHz
Duty Cycle $_{BCLK}$	Bit clock duty cycle	--	0.4	0.5	0.6	--
$T_{BCLK\ rise/fall}$	PCM_CLK rise/fall time	--	--	3	--	ns
$T_{DO}$	Delay from PCM_CLK rising edge to PCM_DOUT rising edge	--	--	--	15	ns
$T_{DISU}$	Setup time for PCM_DIN before PCM_CLK falling edge	--	20	--	--	ns
$T_{DIHO}$	Hold time for PCM_DIN after PCM_CLK falling edge	--	15	--	--	ns
$T_{BF}$	Delay from PCM_CLK rising edge to PCM_SYNC rising edge	--	--	--	15	ns

**Slave mode**



Symbol	Parameter	Condition	Min	Typ	Max	Unit
$F_{BCLK}$	Bit clock frequency	--	--	2/2.048	--	MHz
Duty Cycle $_{BCLK}$	Bit clock duty cycle	--	0.4	0.5	0.6	--
$T_{BCLK\ rise/fall}$	PCM_CLK rise/fall time	--	--	3	--	ns
$T_{DO}$	Delay from PCM_CLK rising edge to PCM_DOUT rising edge	--	--	--	30	ns
$T_{DISU}$	Setup time for PCM_DIN before PCM_CLK falling edge	--	15	--	--	ns
$T_{DIHO}$	Hold time for PCM_DIN after PCM_CLK falling edge	--	10	--	--	ns
$T_{BFSU}$	Setup time for PCM_SYNC before PCM_CLK falling edge	--	15	--	--	ns
$T_{BFHO}$	Hold time for PCM_SYNC after PCM_CLK falling edge	--	10	--	--	ns

# 7 Reference Design



C11, C12, C14 should be placed close to pin 36 of the module  
C13, C15 should be placed close to pin 34 of the module

Module requires independent power supply with VCC\_3V3 current  $\geq 1A$ . Do not share power with amplifier, infrared device, camera, etc. And please pay attention to the power up sequence requirements in part 6.1.

# 8 Ordering Information

Part No.	Description
FGL287BSRX-01	88W8987-A2-NYEE, a/b/g/n/ac, Wi-Fi, BT5.0, 1T1R, SDIO+UART, 2 Antenna version, PCB V2.0, 13x15mm



## 9 The Key Material List

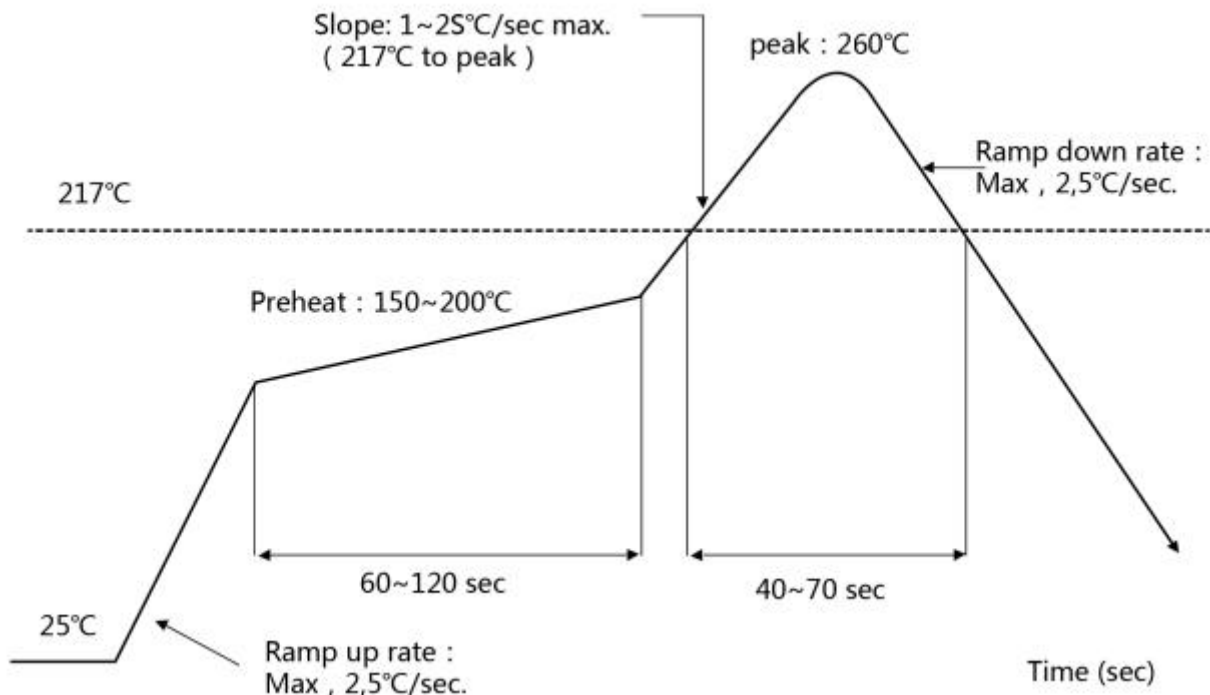
Item	Part Name	Description	Manufacturer
1	Inductor	2016 2.2uH, ±20%	Sunlord, Ceaiya, Cenker, TAIYO YUDEN
2	Diplexer	1608 Dual-band, dual-mode 2.4GHz/5GHz WLAN	Glead, Walsin, ACX, Murata, MAG.LAYERS
3	Crystal	2016 38.4MHz	ECEC, TKD, Hosonic, JWT, TXC
4	Chipset	88W8987-A2-NYEE	NXP
5	PCB	FR4, GREEN	GDKX, Brain-power, Sunlord, Piotech

## 10 Recommended Reflow Profile

Referred to IPC/JEDEC standard.

Peak Temperature : ≤260°C

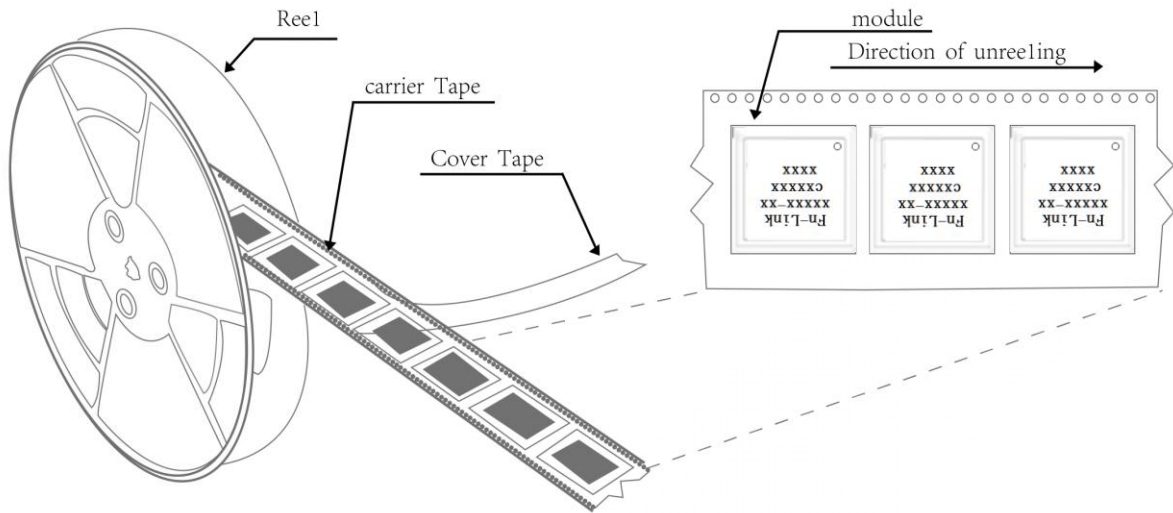
Number of Times : ≤2 times



# 11 Package Information

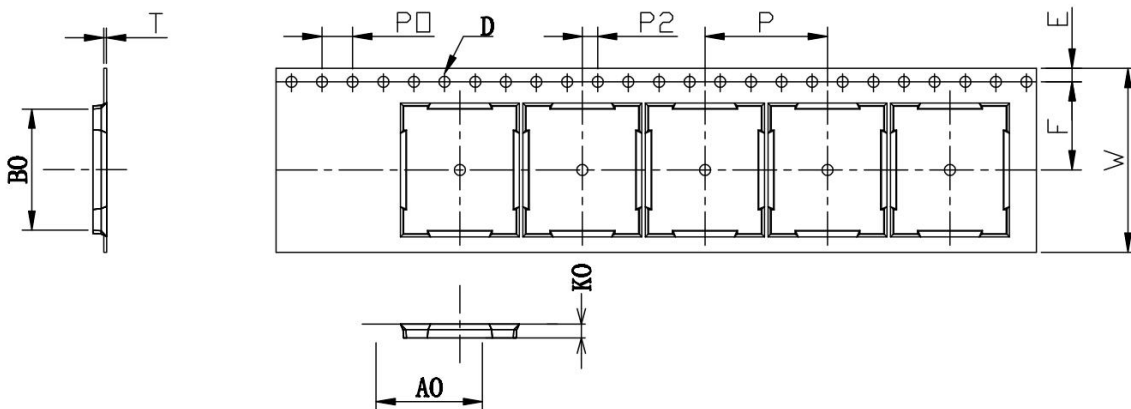
## 11.1 Reel

A roll of 1500pcs

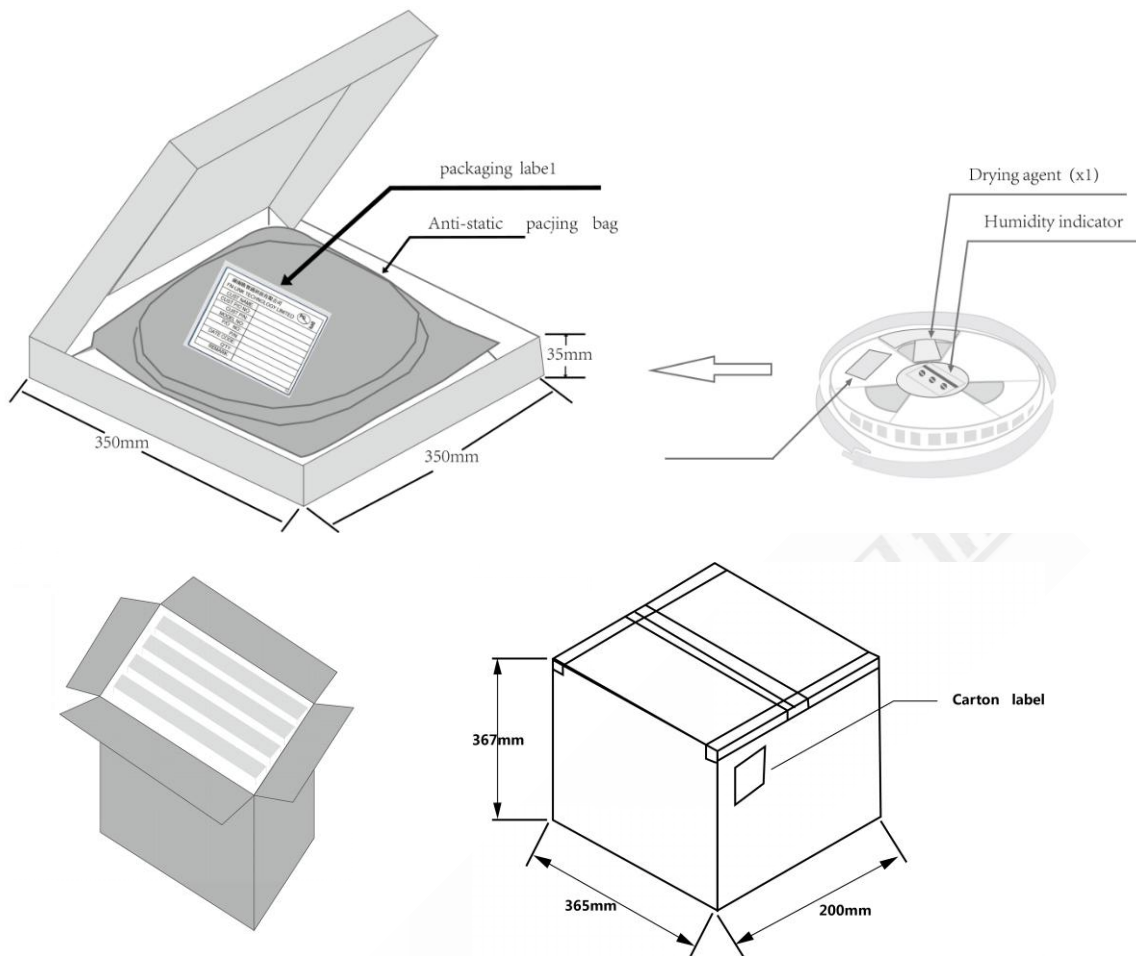


## 11.2 Carrier Tape Detail

ITEM	W	A0	B0	D	F	E	K0	P0	P2	P	T
DIM	24	13.40	15.40	1.50	11.5	1.75	2.65	4.0	2.0	16.0	0.30
TOLE	+0.3 -0.3	±0.15	±0.15	+0.1 -0.0	+0.1 -0.1	±0.1	±0.10	±0.1	±0.1	±0.1	±0.05



### 11.3 Packaging Detail



### 11.4 Moisture sensitivity

The Modules is a Moisture Sensitive Device level 3, in according with standard IPC/JEDEC J-STD-020, take care

all the relatives requirements for using this kind of components.

Moreover, the customer has to take care of the following conditions:

- a) Calculated shelf life in sealed bag: 12 months at <math><40^{\circ}\text{C}</math> and <math><90\%</math> relative humidity (RH).
- b) Environmental condition during the production: - c) The maximum time between the opening of the sealed bag and the reflow process must be 168 hours if condition
- b) "IPC/JEDEC J-STD-033A paragraph 5.2" is respected
- d) Baking is required if conditions b) or c) are not respected
- e) Baking is required if the humidity indicator inside the bag indicates 10% RH or more