FN-LINK欧智通

PRODUCT SPECIFICATION

6192A-SF

Wi-Fi Single-band 2x2 11n Module Datasheet

Version:v1.1

6192A-SF Module Datasheet

	Part NO.	Description
Ordering Information	FG6192ASFX-00	RTL8192FS,b/g/n,Wi-Fi,2T2R,12X12mm,SDIO,with shielding, PCB V1.0
	FG6192ASFX-01	RTL8192FS,b/g/n,Wi-Fi,2T2R,12X12mm,SDIO,no shielding, PCB V1.0

Customer: _____

Customer P/N: _____

Signature: _____

Date: _____

Office: 14th floor, Block B, phoenix zhigu, Xixiang Street, Baoan District, Shenzhen

Factory: NO.8, Litong RD., Liuyang Economic & Technical Development Zone, Changsha, CHINA

TEL:+86-755-2955-8186 Website:www.fn-link.com

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Revision History

Version	Date	Contents of Revision Change	Preparde	Checked	Approved
V1.0	2020/07/22	New version	FC	LXY	QJP
V1.1	2021/12/08	Update the specification format change the standaard to ±2dbm	FC	LXY	QJP
V1.2	2022/03/10	Update -01 type model	FC	LXY	QJP

1. General Description

1.1 Introduction

6192A-SF base on RTL8192FS complied with IEEE 802.11 b/g/n standard from 2.4G-2.5GHz. Support 300Mbps high speed wireless network connection with SDIO interface (1.1/2.0/3.0 compliant).

1.2 Description

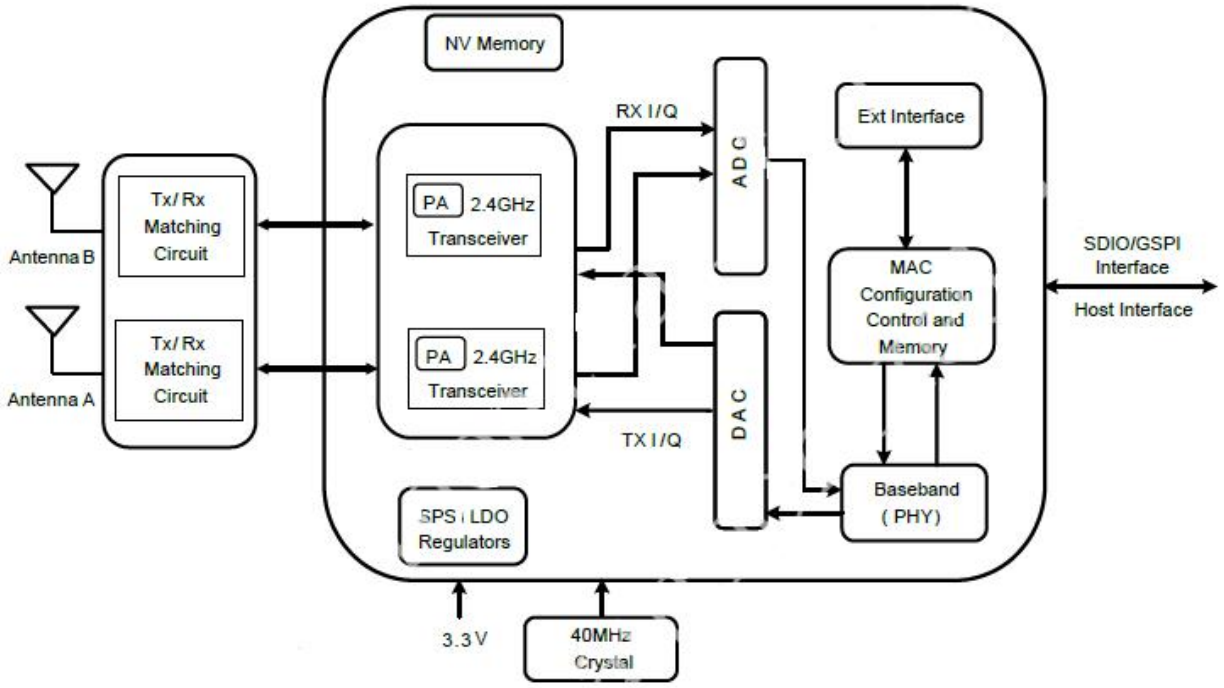
Model Name	6192A-SF
Product Description	Support Wi-Fi functionalities
Dimension	L x W x H: 12 x 12 x1.6 mm
Wi-Fi Interface	Support SDIO V1.1/2.0/3.0
OS supported	Android /Linux/ Win CE /iOS /XP/WIN7/WIN10
Operating temperature	0°C to 70°C
Storage temperature	-40°C to 85°C

2. Features

General

- 12x12mm, 44pin, 3.3V power in
- RTL8192FS.
- Complete 802.11n 2x2 MIMO solution for 2.4GHz, maximum data rate up to 300Mbps using 40Mhz bandwidth
- Complies with SDIO 1.1/2.0/3.0 for WLAN with clock rate up to 100Mhz

3. Block Diagram



4. General Specification

4.1 WI-FI Specification

Feature	**Description**	
WLAN Standard	IEEE 802.11 b/g/n Wi-Fi compliant	
Frequency Range	2.400 GHz ~ 2.497 GHz (2.4 GHz ISM Band)	
Number of Channels	2.4GHz：Ch1 ~ Ch14	
Modulation	DBPSK/DQPSK/CCK(DSSS) BPSK/QPSK/16QAM/64QAM(OFDM)	
Test Items	**Typical Value**	**EVM**
Output Power	802.11b /11Mbps : 18dBm ± 2 dB	EVM ≤ -9dB
	802.11g /54Mbps : 16dBm ± 2 dB	EVM ≤ -26dB
	802.11n /MCS7 : 15dBm ± 2 dB	EVM ≤ -28dB
Spectrum Mask	Meet with IEEE standard	

Freq. Tolerance	±20ppm		
Receive Sensitivity (11b,20MHz) @8% PER	- 1Mbps	PER @ -88 dBm	≤-83
	- 2Mbps	PER @ -87 dBm	≤-80
	- 5.5Mbps	PER @ -85 dBm	≤-79
	- 11Mbps	PER @ -82 dBm	≤-76
Receive Sensitivity (11g,20MHz) @10% PER	- 6Mbps	PER @ -86 dBm	≤-85
	- 9Mbps	PER @ -85 dBm	≤-84
	- 12Mbps	PER @ -84 dBm	≤-82
	- 18Mbps	PER @ -82 dBm	≤-80
	- 24Mbps	PER @ -80 dBm	≤-77
	- 36Mbps	PER @ -77 dBm	≤-73
	- 48Mbps	PER @ -73 dBm	≤-69
	- 54Mbps	PER @ -71 dBm	≤-65
Receive Sensitivity (11n,20MHz) @10% PER	- MCS=0	PER @ -83 dBm	≤-82
	- MCS=1	PER @ -82 dBm	≤-79
	- MCS=2	PER @ -80 dBm	≤-77
	- MCS=3	PER @ -78 dBm	≤-74
	- MCS=4	PER @ -75 dBml	≤-70
	- MCS=5	PER @ -71 dBm	≤-66
	- MCS=6	PER @ -69 dBm	≤-65
	- MCS=7	PER @ -67 dBm	≤-64
Receive Sensitivity (11n,40MHz) @10% PER	- MCS=0	PER @ -82 dBm	≤-79
	- MCS=1	PER @ -81 dBm	≤-76
	- MCS=2	PER @ -80 dBm	≤-74
	- MCS=3	PER @ -76 dBm	≤-71
	- MCS=4	PER @ -72 dBm	≤-67
	- MCS=5	PER @ -68 dBm	≤-63
	- MCS=6	PER @ -66 dBm	≤-62
	- MCS=7	PER @ -65 dBm	≤-61

5. ID setting information

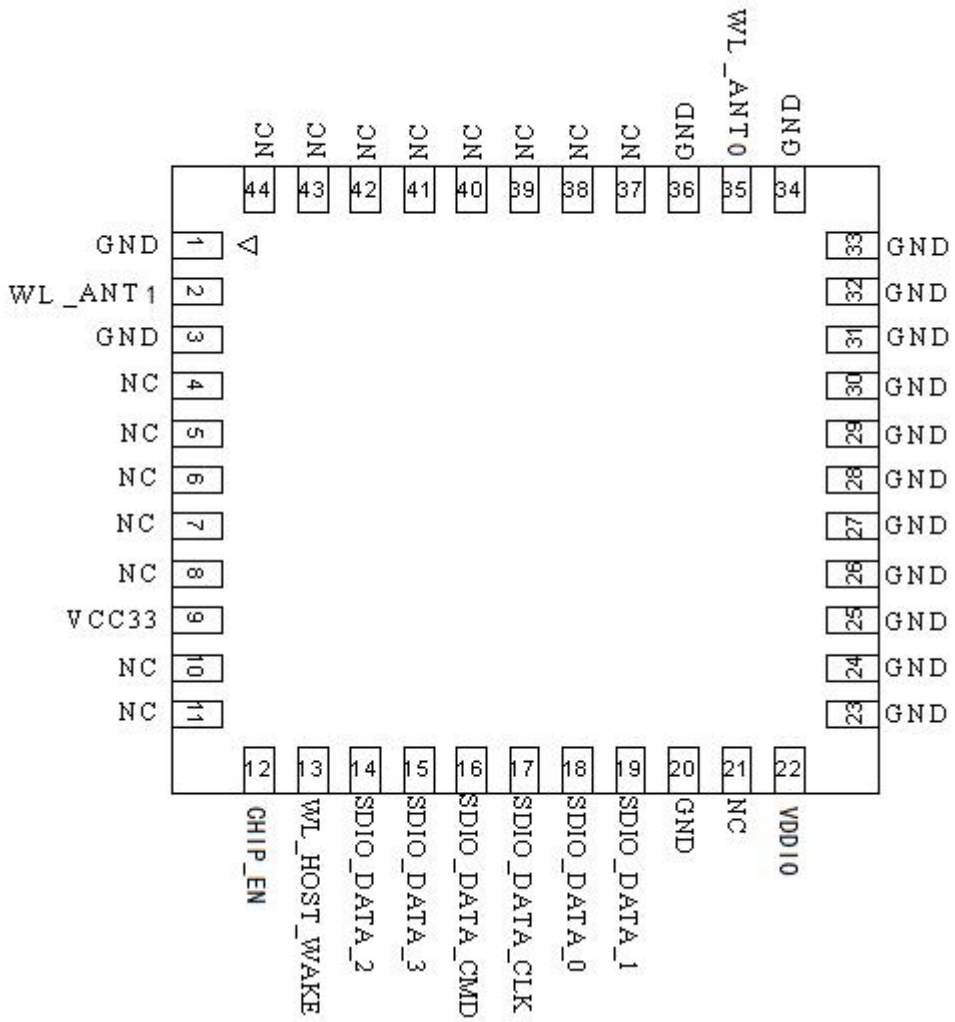
WI-FI

Vendor ID	-
Product ID	-

6. Pin Definition

6.1 Pin Outline

< TOP VIEW



6.2 Pin Definition details

NO.	Name	Type	Description	Voltage
1	GND	—	Ground connections	
2	WL_ANT 1	I/O	RF I/O port1	
3	GND	—	Ground connections	
4	NC	—	Floating (Don’t connected to ground)	
5	NC	—	Floating (Don’t connected to ground)	
6	NC	—	Floating (Don’t connected to ground)	
7	NC	—	Floating (Don’t connected to ground)	
8	NC	—	Floating (Don’t connected to ground)	
9	VCC33	P	Main power voltage source input 3.3V	3.3V
10	NC	—	Floating (Don’t connected to ground)	
11	NC	—	Floating (Don’t connected to ground)	
12	CHIP_EN	I	Enable pin for Chip ON: default pull high ; OFF: external pull low	3.3V
13	WLAN_HOST_WAKE	O	wake-up function	3.3V
14	SDIO_DATA_2	I/O	SDIO data line 2	VDDIO
15	SDIO_DATA_3	I/O	SDIO data line 3	VDDIO
16	SDIO_DATA_CMD	I/O	SDIO command line	VDDIO
17	SDIO_DATA_CLK	I/O	SDIO clock line	VDDIO
18	SDIO_DATA_0	I/O	SDIO data line 0	VDDIO
19	SDIO_DATA_1	I/O	SDIO data line 1	VDDIO
20	GND	—	Ground connections	
21	NC	—	Floating (Don’t connected to ground)	
22	VDDIO	I	VDDIO power	1.8V or 3.3V
23	GND	—	Ground connections	
24	GND	—	Ground connections	
25	GND	—	Ground connections	
26	GND	—	Ground connections	
27	GND	—	Ground connections	
28	GND	—	Ground connections	
29	GND	—	Ground connections	
30	GND	—	Ground connections	
31	GND	—	Ground connections	
32	GND	—	Ground connections	
33	GND	—	Ground connections	
34	GND	—	Ground connections	

35	WL_ANT 0	—	RF I/O port0	
36	GND	—	Ground connections	
37	NC	—	Floating (Don't connected to ground)	
38	NC	—	Floating (Don't connected to ground)	
39	NC	—	Floating (Don't connected to ground)	
40	NC	—	Floating (Don't connected to ground)	
41	NC	—	Floating (Don't connected to ground)	
42	NC	—	Floating (Don't connected to ground)	
43	NC	—	Floating (Don't connected to ground)	
44	NC	—	Floating (Don't connected to ground)	

P:POWER I:INPUT O:OUTPUT VDDIO:1.8V or 3.3V

7. Electrical Specifications

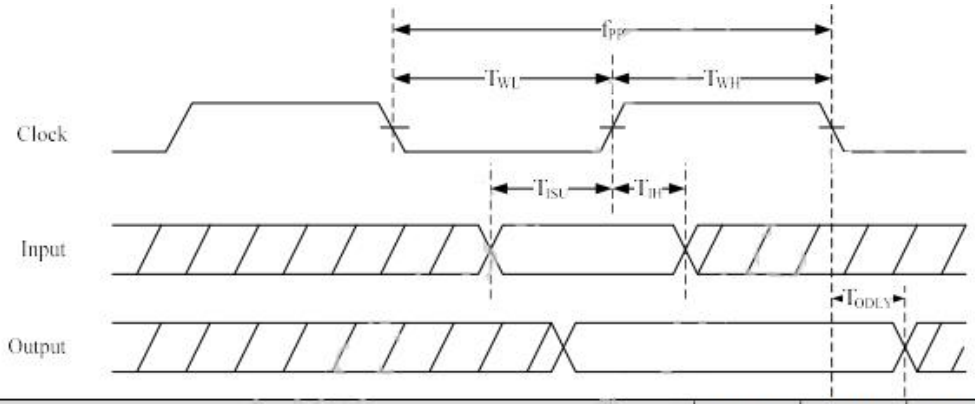
7.1 Power Supply DC Characteristics

The digital IO supports VDD33 or VDD18 application.

	MIN	TYP	MAX	Unit
Operating Temperature	0	25	70	deg.C
VCC33	3.0	3.3	3.6	V
VDDIO	1.7	1.8 or 3.3	3.6	V

7.2 Interface Circuit time series

7.2.1 SDIO interface timing



NO	Parameter	Mode	MIN	MAX	Unit
f_{PP}	Clock frequency	Default	0	25	MHz
		HS	0	50	MHz
T_{WL}	Clock low time	DEF	10		ns
		HS	7		ns
T_{WH}	Clock high time	DEF	10		ns
		HS	7		
T_{ISU}	Input setup time	DEF	5		ns
		HS	6		
T_{IH}	Input hold time	DEF	5		ns
		HS	2		
T_{ODLY}	Output delay time	DEF		14	ns
		HS		14	

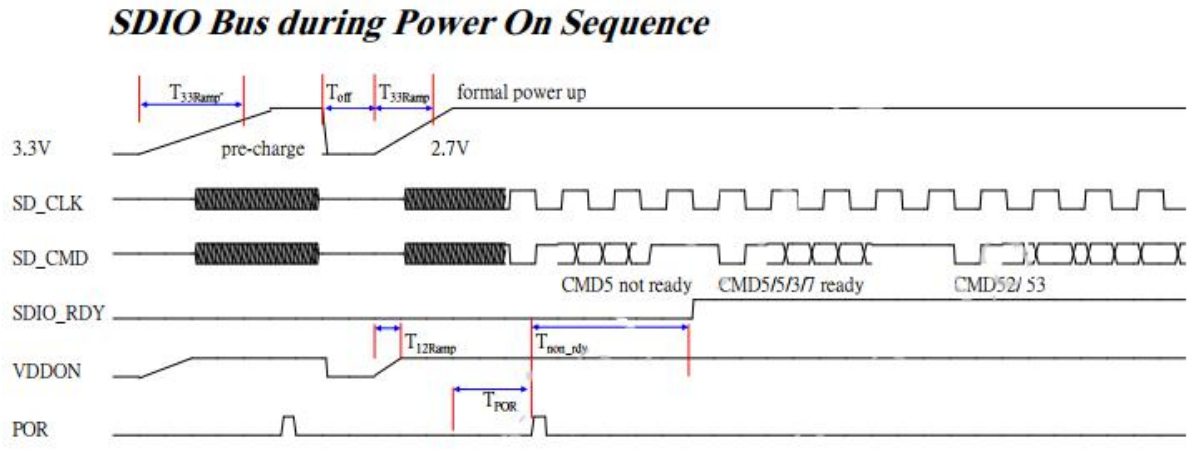


Figure 3. RTL8192FS SDIO Bus Power On Sequence

T_{33ramp}': The 3.3V power pre-charge ramp up duration before formal power up. It is recommended that a 3.3V power on and then power off sequence is executed by host controller before the formal power on sequence. This procedure can eliminate the host card detection issue when power ramp up duration is too long or the system warm reboot failure issue.

T_{off} : The duration the 3.3V is cut off before formal power up.

T_{33ramp}: The 3.3V main power ramp up duration

T_{12ramp}: The internal 1.2V ramp up duration.

T_{POR}: The duration the power on reset releases and power management unit executes power on tasks. The power on reset will detect both 3.3V and 1.2V power ramp up and after a predetermined duration.

T_{non_rdy}: SDIO not ready duration, in this state, card may respond command without ready bit set. After ready bit set, host will initiate complete card detection procedure.

Table 10. The typical timing range

	Min	Typical	Max	Unit
T_{33ramp}'	0.2	0.5	2.5	ms
T_{off}	250	500	1000	ms
T_{33ramp}	0.2	0.5	2.5	ms
T_{12ramp}	0.1	0.5	1.5	ms
T_{por}	2	2	8	ms
$T_{non-rdy}$	1	2	10	ms

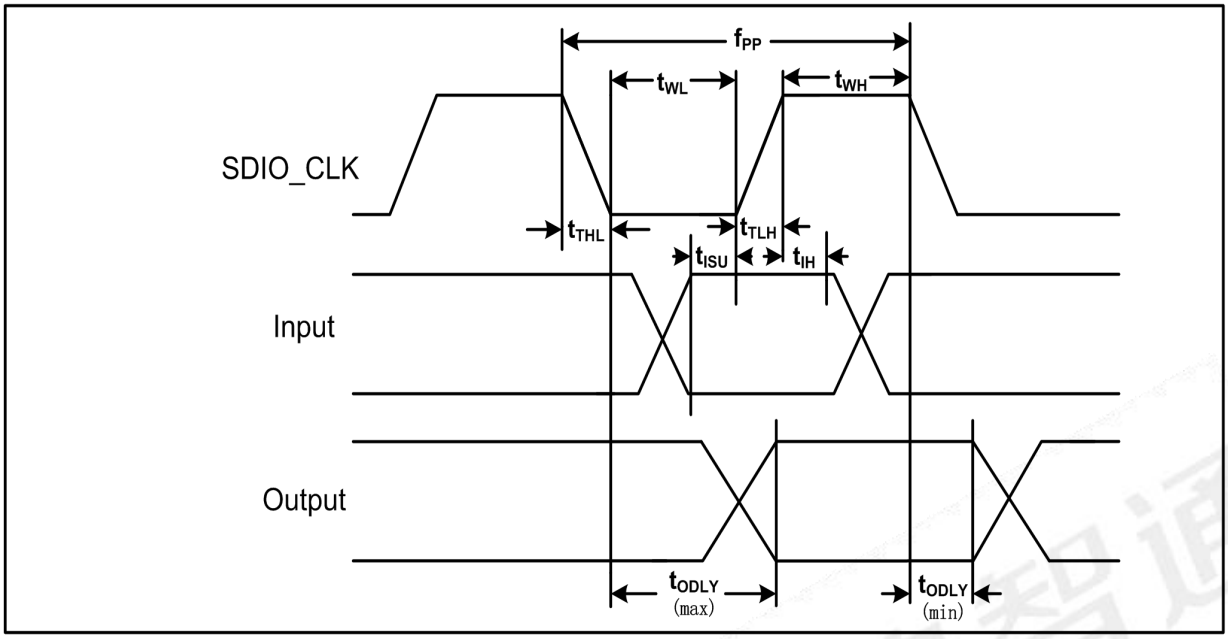
7.2.2 SDIO Pin Description

The module supports SDIO version 3.0, signal level ranges from 1.8V to 3.3V.

SDIO Pin Description

SD 4-Bit Mode	
DATA0	Data Line 0
DATA1	Data Line 1 or Interrupt
DATA2	Data Line 2 or Read Wait
DATA3	Data Line 3
CLK	Clock
CMD	Command Line

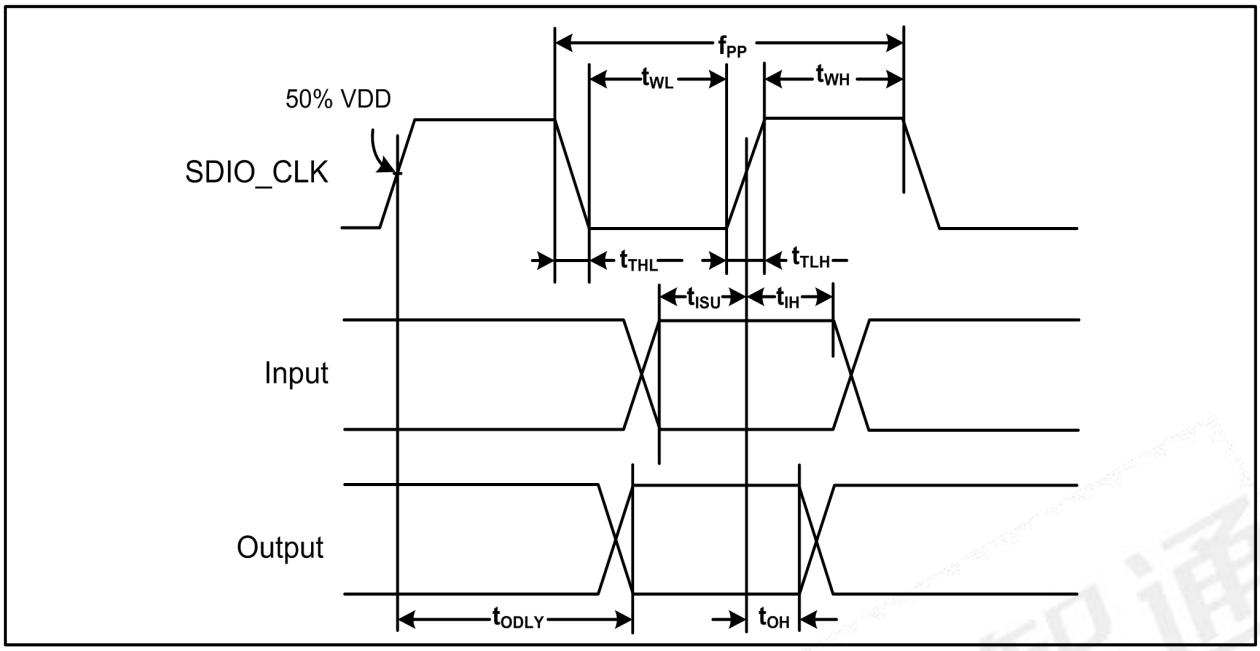
7.2.3 SDIO Default Mode Timing Diagram



Parameter	*Symbol*	*Minimum*	*Typical*	*Maximum*	*Unit*
SDIO CLK(All values are referred to minimum VIH and maximum VIL[b])					
Frequency - Data Transfer mode	fPP	0	-	25	MHz
Frequency - Identification mode	fOD	0	-	400	kHz
Clock low time	tWL	10	-	-	ns
Clock high time	tWH	10	-	-	ns
Clock rise time	tTLH	-	-	10	ns
Clock low time	tTHL	-	-	10	ns
Inputs:CMD, DAT(referenced to CLK)					
Input setup time	tISU	5	-	-	ns
Input hold time	tIH	5	-	-	ns
Outputs:CMD, DAT(referenced to CLK)					
Output delay time - Data Transfer mode	tODLY	0	-	14	ns
Output delay time - Identification mode	tODLY	0	-	50	ns

a. Timing is based on CL ≤ 40 pF load on CMD and Data.

b. Min(Vih) = 0.7 × VDDIO and max(Vil) = 0.2 × VDDIO.



7.2.4 SDIO High Speed Mode Timing Diagram

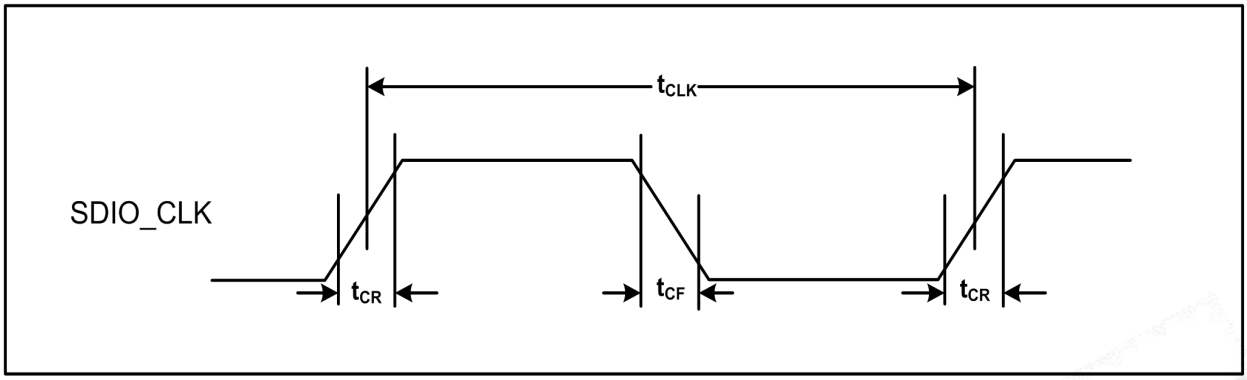
Parameter	*Symbol*	*Minimum*	*Typical*	*Maximum*	*Unit*
SDIO CLK(all values are referred to minimum VIH and maximum VIL[b])					
Frequency - Data Transfer mode	fPP	0	-	50	MHz
Frequency - Identification mode	fOD	0	-	400	kHz
Clock low time	tWL	7	-	-	ns
Clock high time	tWH	7	-	-	ns
Clock rise time	tTLH	-	-	3	ns
Clock low time	tTHL	-	-	3	ns
Inputs:CMD, DAT(referenced to CLK)					
Input setup time	tISU	6	-	-	ns
Input hold time	tIH	2	-	-	ns
Outputs:CMD, DAT(referenced to CLK)					
Output delay time - Data Transfer mode	tODLY	-	-	14	ns
Output delay time - Identification mode	tODLY	2.5	-	-	ns
Total system capacitance(each line)	CL	-	-	40	pF

a. Timing is based on CL ≤ 40 pF load on CMD and Data.

b. Min(Vih) = 0.7 × VDDIO and max(Vil) = 0.2 × VDDIO.

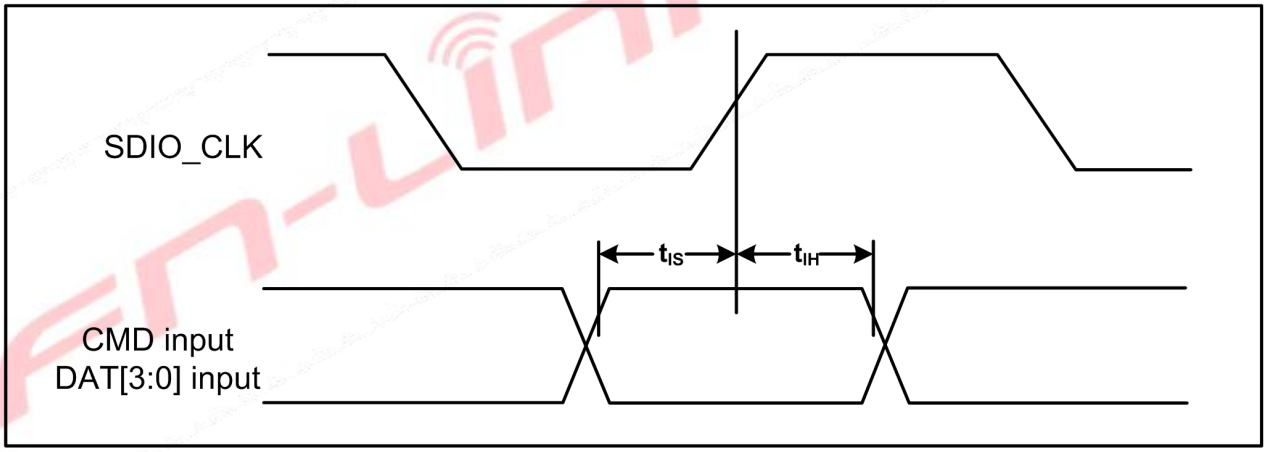
7.2.5 SDIO Bus Timing Specifications in SDR Modes

Clock timing(SDR Modes)



Parametwer	*Symbol*	*Minimum*	*Maximum*	*Unit*	*Comments*
-	t_{CLK}	40	-	ns	SDR12 mode
		20	-	ns	SDR25 mode
		10	-	ns	SDR50 mode
-	t_{CR}, t_{CF}	-	0.2 × t_{CLK}	ns	t_{CR}, t_{CF} < 2.00 ns (max)@100 MHz, C_{CARD} = 10 pF
Clock duty	-	30	70	%	-

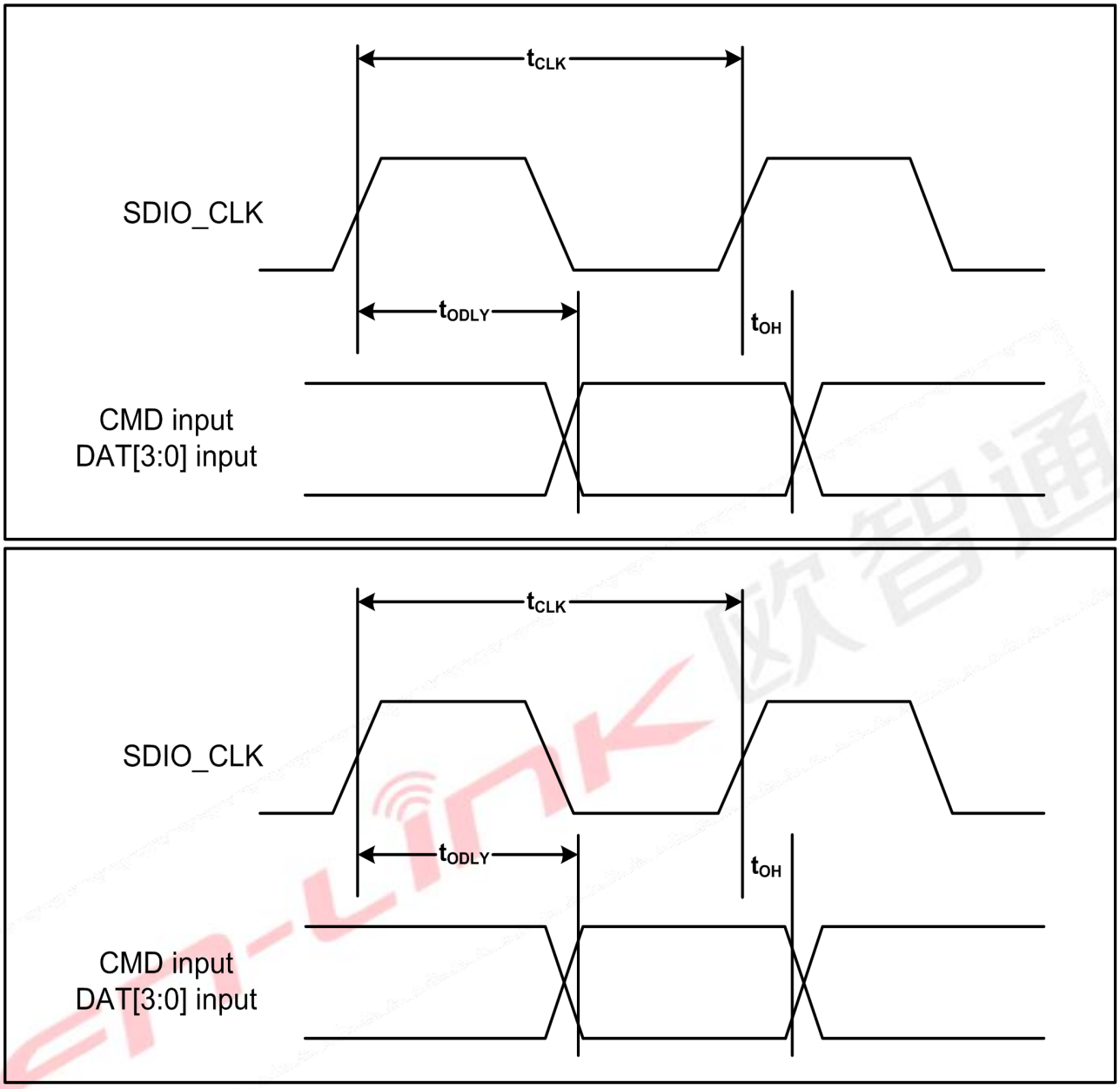
Card Input timing (SDR Modes)



Symbol	*Minimum*	*Maximum*	*Unit*	*Comments*
SDR50 Mode				
t_{IS}	3.00	-	ns	C_{CARD} = 10pF, VCT = 0.975V
t_{IH}	0.80	-	ns	C_{CARD} = 5pF, VCT = 0.975V

a. SDIO 3.0 specification value is 1.40 ns.

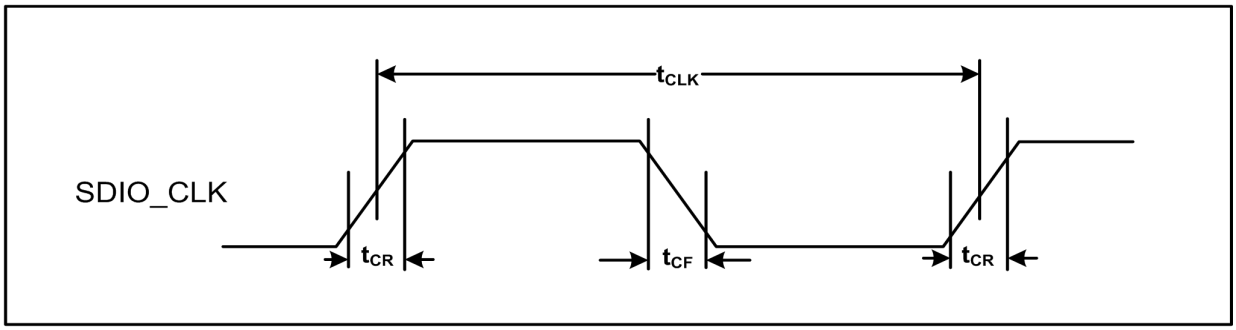
Card output timing (SDR Modes up to 100MHz)



Symbol	*Minimum*	*Maximum*	*Unit*	*Comments*
t_{ODLY}	-	7.85[a]	ns	t_{CLK}≥10 ns C_L=30 pF using driver type B for SDR50
t_{ODLY}	-	14.0	ns	t_{CLK}≥20 ns C_L=40 pF using for SDR12, SDR25
t_{OH}	1.5	-	ns	Hold time at the t_{ODLY}(min) CL=15 pF

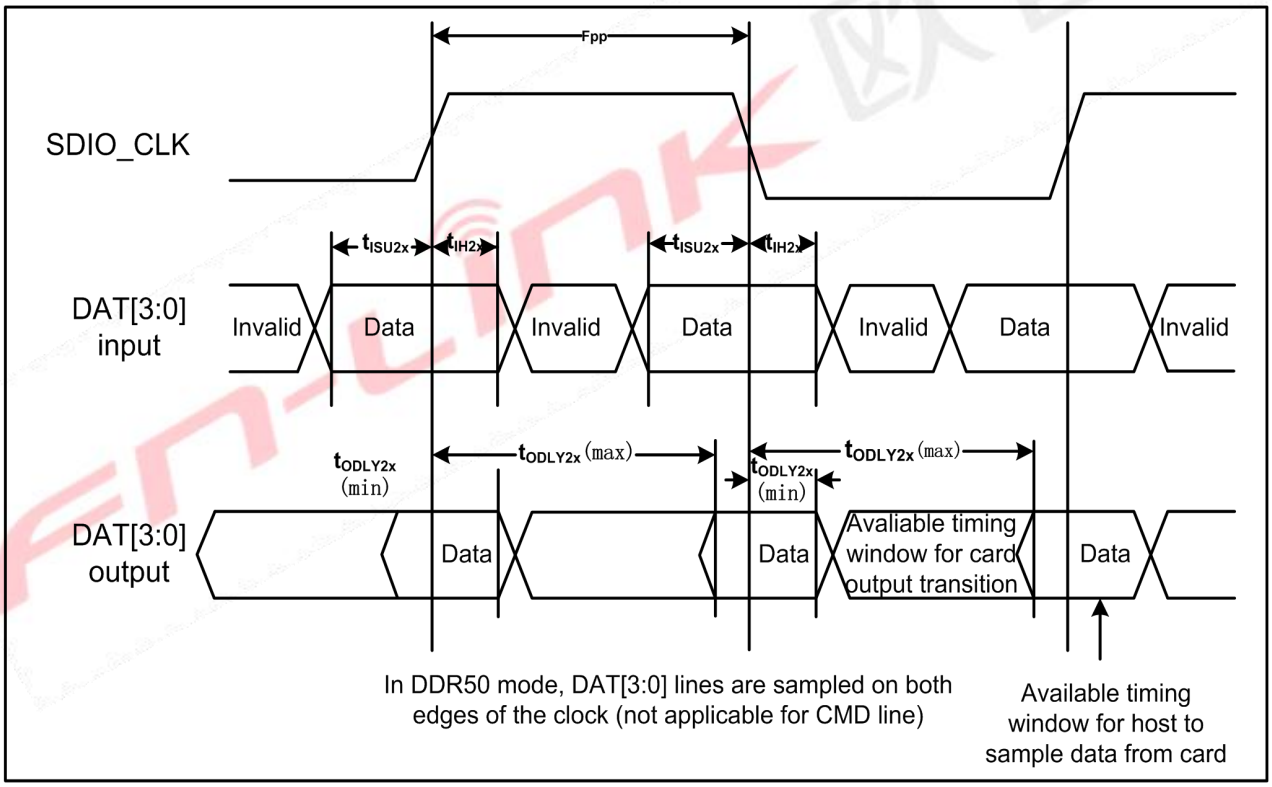
a. SDIO 3.0 specification value is 7.5 ns.

7.2.6 SDIO Bus Timing Specifications in DDR50 Mode



parameter	*Symbol*	*Minimum*	*Maximum*	*Unit*	*Comments*
-	t_{CLK}	20	-	ns	DDR50 mode
-	t_{CR}, t_C	-	0.2 ×t_{CLK}	ns	t_{CR}, t_{CF} < 4.00 ns (max)@50 MHz, C_{CARD} = 10 pF
Clock duty	-	45	55	%	-

Data Timing



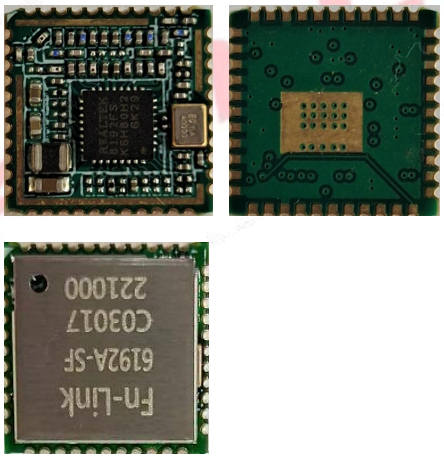
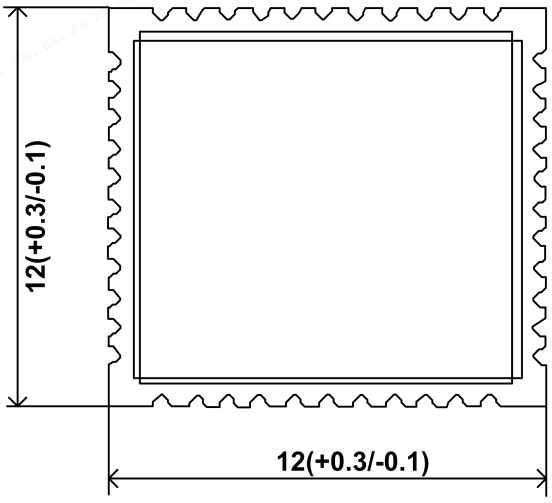
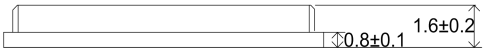
parameter	*Symbol*	*Minimum*	*Maximum*	*Unit*	*Comments*
Input CMD					
Input setup time	t_{ISU}	6	-	ns	C_{CARD} < 10 pF (1 Card)
Input hold time	t_{IH}	0.8	-	ns	C_{CARD} < 10 pF (1 Card)
Output CMD					

Output delay time	t_{ODLY}	-	13.7	ns	C_{CARD} < 30 pF (1 Card)
Output hold time	t_{OH}	1.5	-	ns	C_{CARD} < 15 pF (1 Card)
Input DAT					
Input setup time	t_{ISU2x}	3	-	ns	C_{CARD} < 10 pF (1 Card)
Input hold time	t_{IH2x}	0.8	-	ns	C_{CARD} < 10 pF (1 Card)
Output CMD					
Output delay time	t_{ODLY2x}	-	7.85[a]	ns	C_{CARD} < 25 pF (1 Card)
Output hold time	t_{ODLY2x}	1.5	-	ns	C_{CARD} < 15 pF (1 Card)

a. SDIO 3.0 specification value is 7.0 ns

8. Size reference

8.1 Module Picture

<table>
<tr><td>L x W : 12 x 12 (+0.3/-0.1) mm
 
</td><td> 
</td></tr>
<tr><td>H: 1.6 (±0.2) mm
H:2.35 (±0.2) mm ---with shielding</td><td> 
</td></tr>
<tr><td>Weight</td><td>0.54g</td></tr>
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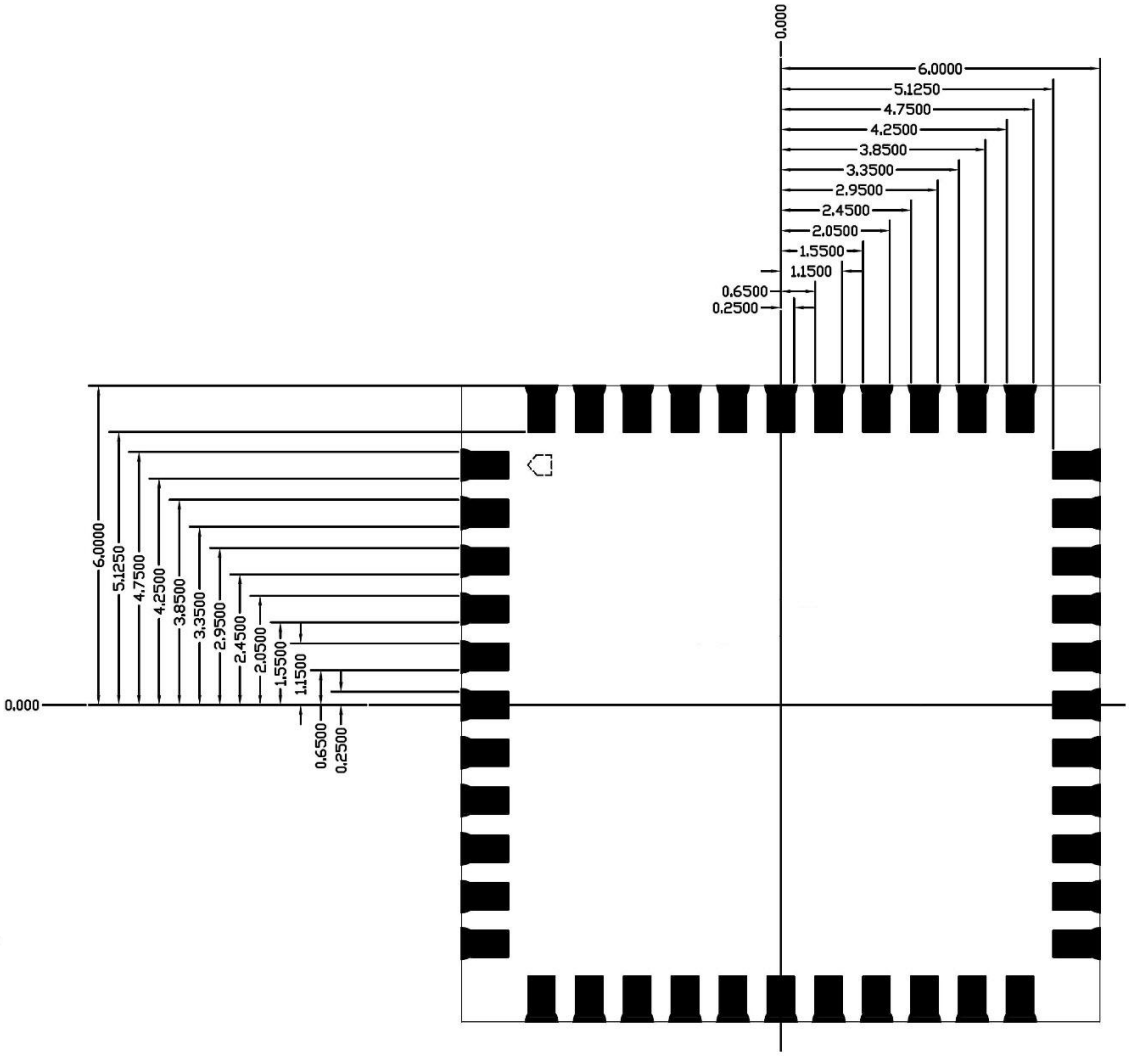
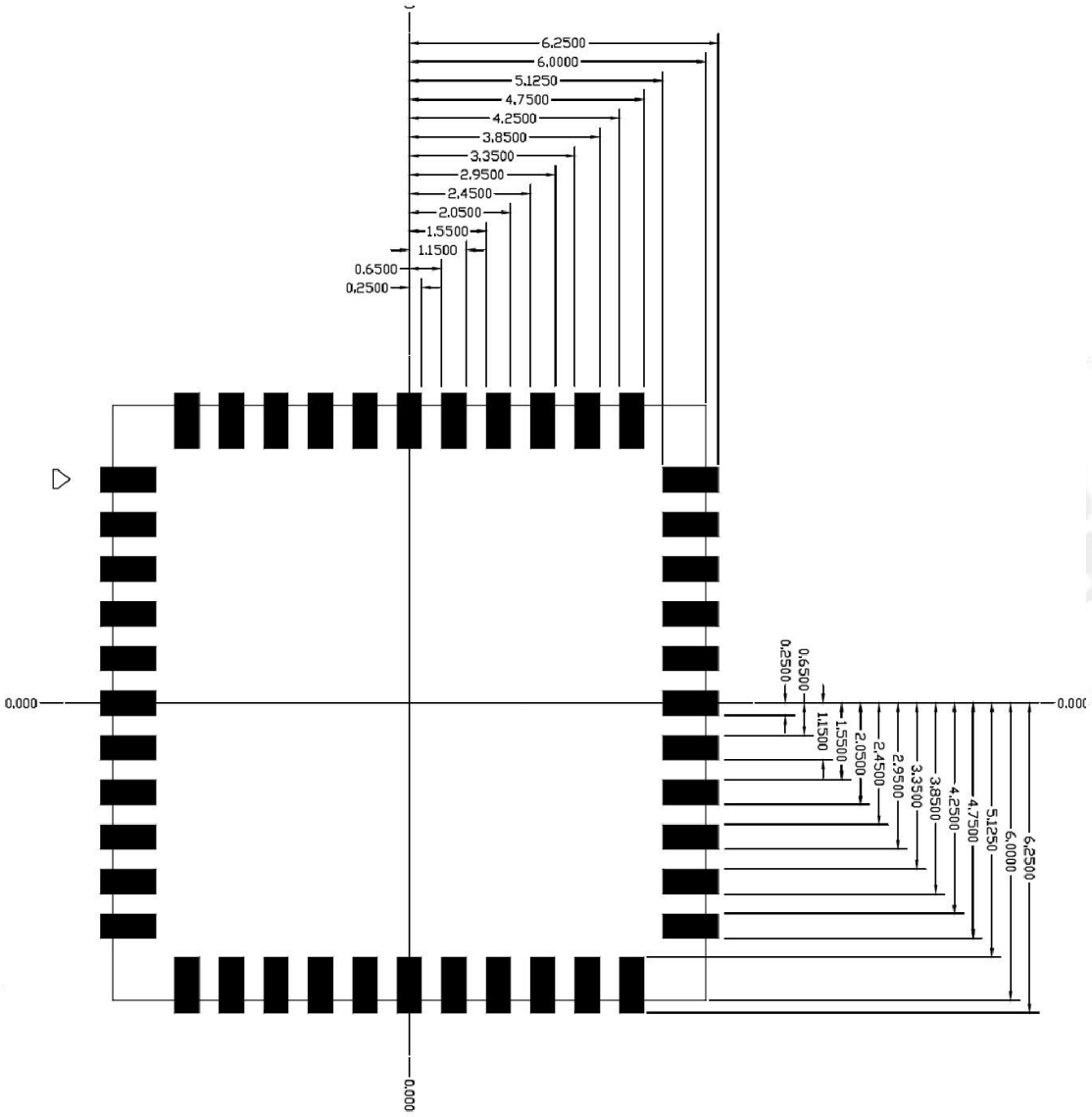
8.2 Physical Dimensions

<TOP View>



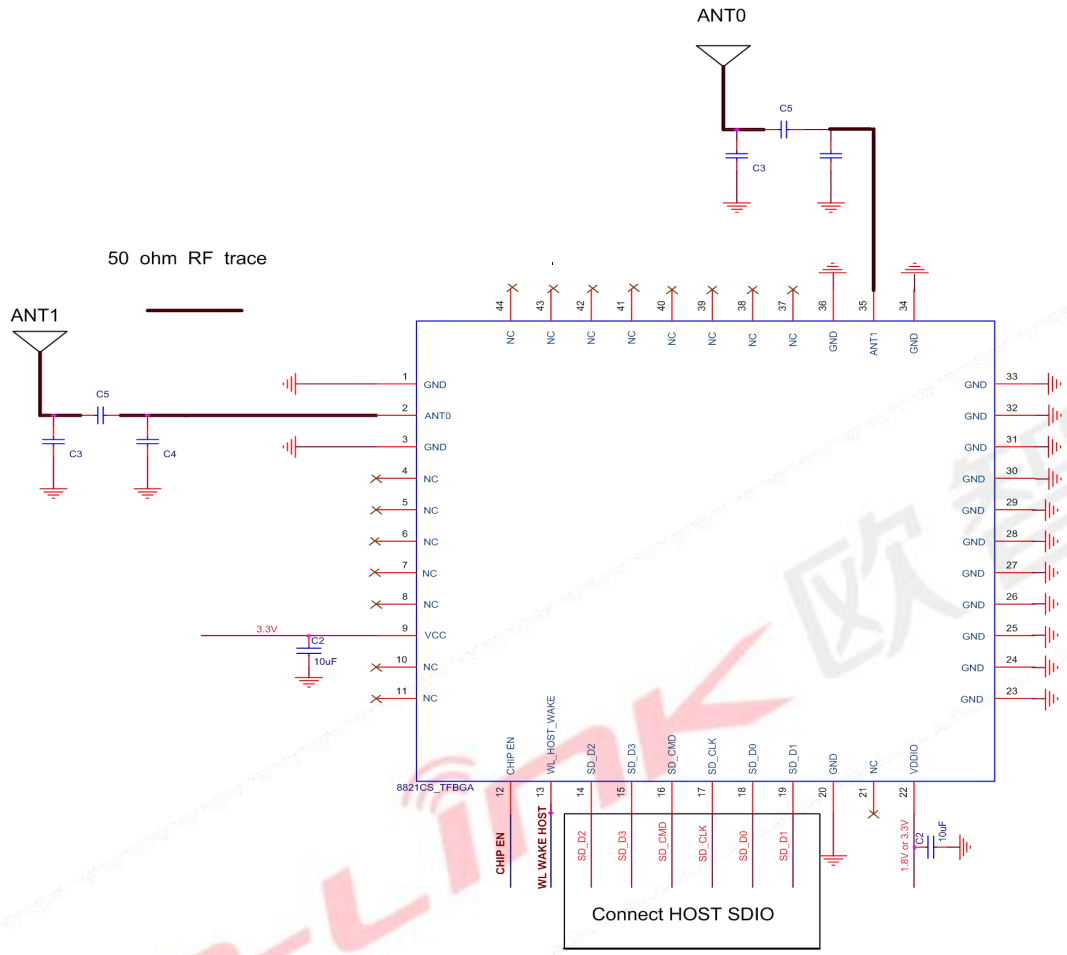
8.3 Layout Recommendation



9. The Key Material List

Name	specification	supplier
Chipset	RTL8192FS-CG QFN-32	Realtek
PCB	6192A-SF 12X12X0.8mm 4L	XY-PCB,KX-PCB,SL-PCB,Sunlord
Crystal	2520 40MHz 10ppm 12PF	TST,HOSONIC,TKD,ECEC,JWT
Inductor	0806 2.2uH,±20%,1200mA	Microgate,sunlord,cenke,ceaiya

10. Reference Design

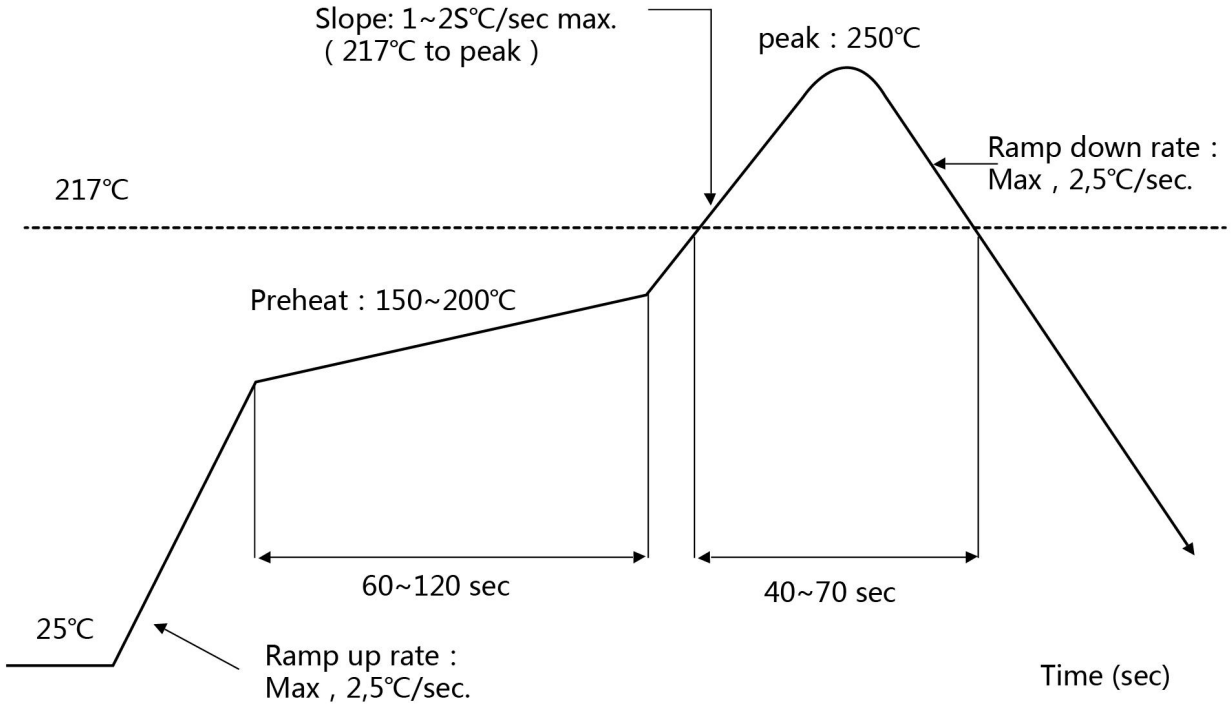


11. Recommended Reflow Profile

Referred to IPC/JEDEC standard.

Peak Temperature : <250°C

Number of Times : ≤2 times



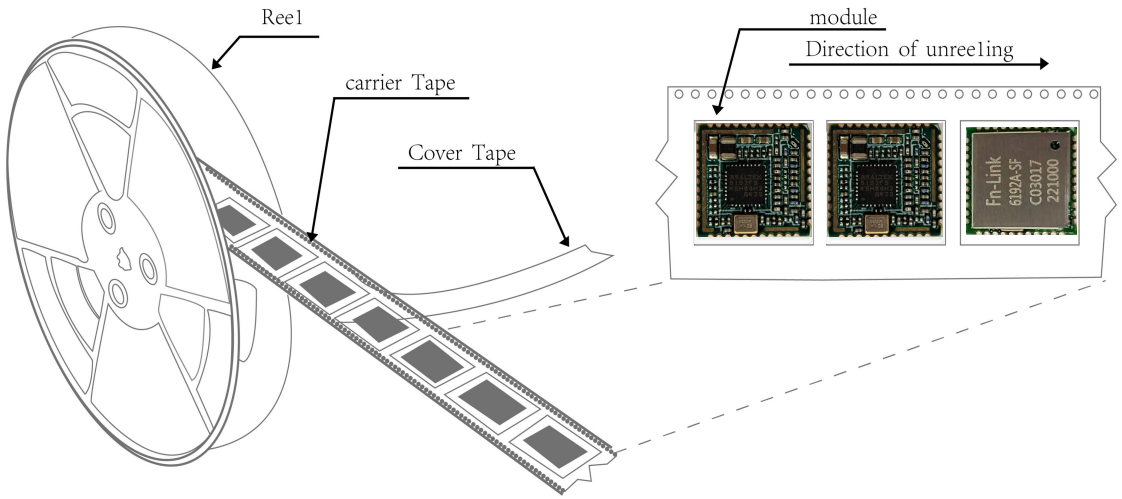
12. RoHS compliance

All hardware components are fully compliant with EU RoHS directive

13. Package

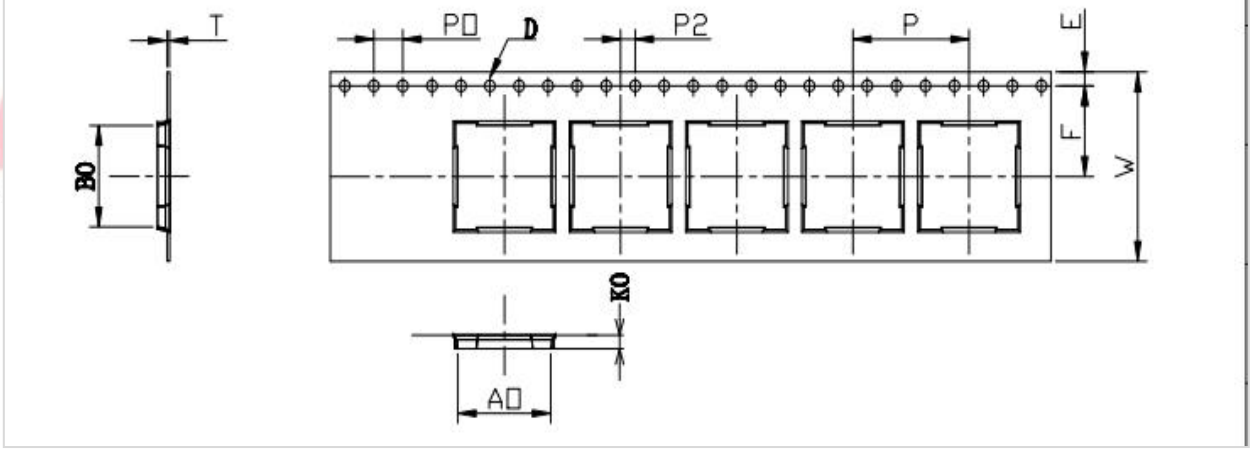
13.1 Reel

A roll of 1500pcs



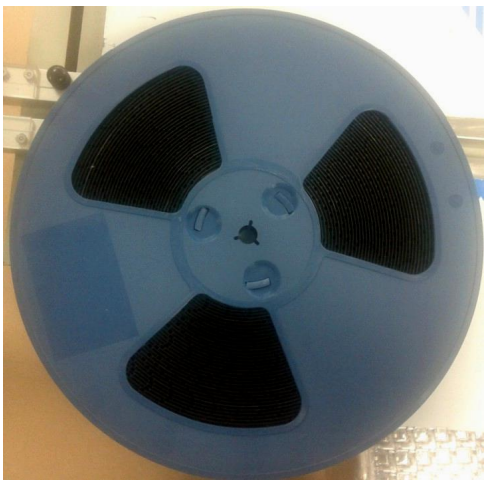
13.2 Carrier Tape Detail

ITEM	W	A0	B0	D	F	E	K0	P0	P2	P	T
DIM	24	12.45	12.45	1.50	11.5	1.75	2.60	4.0	2.0	16.0	0.30
TOLE	+0.3 -0.3	±0.10	±0.10	+0.1 -0.0	+0.1 -0.1	±0.1	±0.10	±0.1	±0.1	±0.1	±0.05



13.3 Packaging Detail

the take-up package



Using self-adhesive tape

Size of black tape: 24mm*32.6m the cover tape :21.3mm*32.6m

Color of plastic disc: blue

NY bag size:460mm*385mm size ： 350*350*35mm

The packing case size:350*210*370mmg

14. Moisture sensitivity

The Modules is a Moisture Sensitive Device level 3, in according with standard IPC/JEDEC J-STD-020, take care
all the relatives requirements for using this kind of components.
Moreover, the customer has to take care of the following conditions:

a) Calculated shelf life in sealed bag: 12 months at <40°C and <90% relative humidity (RH)

b) Environmental condition during the production: 30°C / 60% RH according to IPC/JEDEC J-STD-033A paragraph 5

c) The maximum time between the opening of the sealed bag and the reflow process must be 168 hours if condition

b) "IPC/JEDEC J-STD-033A paragraph 5.2" is respected

d) Baking is required if conditions b) or c) are not respected

e) Baking is required if the humidity indicator inside the bag indicates 10% RH or more