

PRODUCT SPECIFICATION

6223N-SRD

Wi-Fi Single-band 1x1 + Bluetooth 4.2

Combo Module

Version:v1.1



6223N-SRD Module Datasheet

Ordering Information	Part NO.	Description
	FG6223NSRD-00	RTL8723DS,b/g/n,wifi1T1R+BT4.2,21*23.21mm,SDIO+UAR T,with metal antenna.

Customer: _____

Customer P/N: _____

Signature: _____

Date: _____

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Revision History

Version	Date	Contents of Revision Change	Draft	Checked	Approved
V1.0	2020/11/09	New version	FC	LXY	-
V1.1	2022/02/07	1.Update the specification format 2.Up and down electricity time series supplement 3.The RF index was changed to ± 2 dbm 4.Update power supply DC Characteristics and power consumption	FC	LXY	QJP

1. General Description

1.1 Introduction

6223N-SRD is a highly integrated and excellent performance Wireless LAN (WLAN) and BT. It provides SDIO interface for Wi-Fi to connect with host processor and high speed UART interface for BT. High-speed wireless connection up to 150 Mbps and Bluetooth can support BT2.1+EDR/BT3.0 and BT4.2. It can be easily manufactured on SMT process.

This WLAN Module design is based on Realtek RTL8723DS. It combines a MAC, a 1T1R capable baseband, and RF in a single chip. It is designed to provide excellent performance with low power Consumption and enhance the advantages of robust system and cost-effective.

6223N-SRD integrates whole Wi-Fi/BT function blocks into a chip, such as SDIO/UART, MAC, BB, AFE, RFE, PA, EEPROM and LDO/SWR, except fewer passive components remained on PCB.

This compact module is a total solution for a combination of Wi-Fi + BT technologies. The module is specifically developed for Smart phones and Portable devices.

1.2 Description

Model Name	6223N-SRD
Product Description	Support Wi-Fi/Bluetooth functionalities
Dimension	L x W x H: 23 x 21 x 4.8 (typical) mm
Wi-Fi Interface	Support SDIO 2.0
BT Interface	UART
OS supported	Android /Linux/ Win CE /iOS /XP/WIN7/WIN10
Operating temperature	0°C to 70°C
Storage temperature	-40°C to 125°C

2. Features

PHY Features

- Operate at ISM frequency bands (2.4GHz)
- CMOS MAC, Baseband PHY, and RF in a single chip for 802.11b/g/n compatible WLAN
- Wi-Fi 1 transmitter and 1 receiver allow data rates supporting up to 150 Mbps downstream and 150 Mbps upstream PHY rates

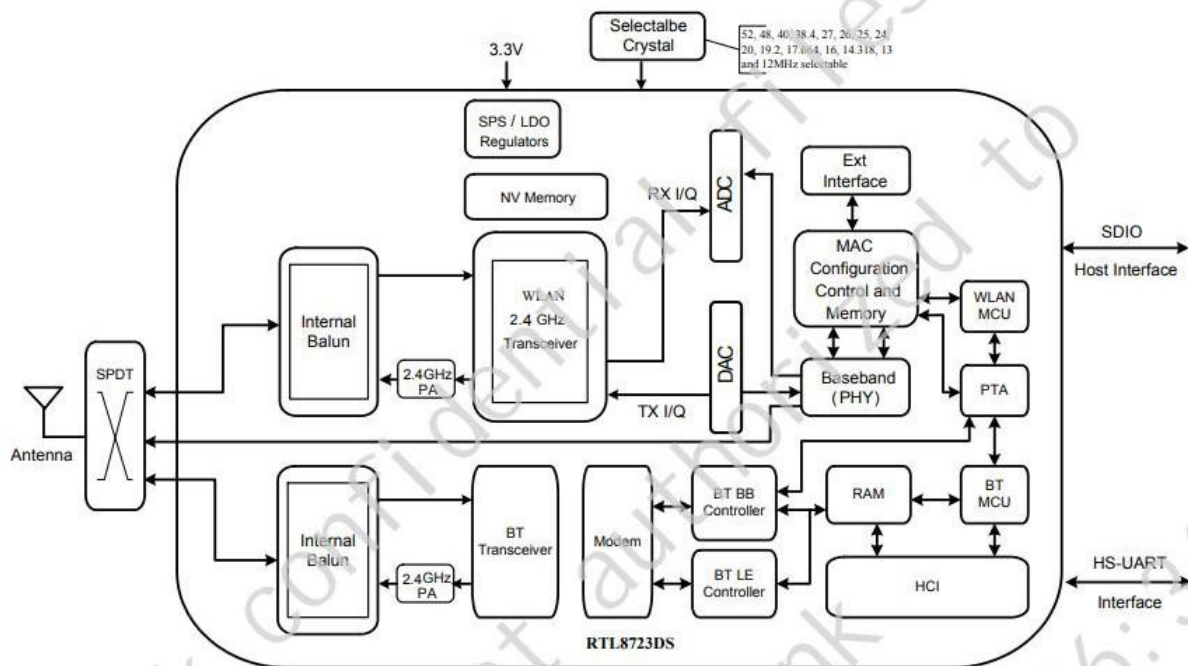
Host Interface

- SDIO1.1/2.0 for Wi-Fi and UART for Bluetooth

Bluetooth Features

- Fully Qualified for Bluetooth 2.1+EDR specification including both 2Mbps and 3Mbps modulation mode
- Fully qualified for Bluetooth 3.0
- Fully qualified for Bluetooth 4.2 Dual mode
- Full_speed Bluetooth operation with Piconet and Scatternet support

3. Block Diagram



4. General Specification

4.1 WI-FI Specification

Feature	Description	
WLAN Standard	IEEE 802.11 b/g/n Wi-Fi compliant	
Frequency Range	2.400 GHz ~ 2.497 GHz (2.4 GHz ISM Band)	
Number of Channels	2.4GHz: Ch1 ~ Ch13	
Test Items	Typical Value	EVM
Output Power	802.11b /11Mbps : 17dBm ± 2 dB	EVM ≤ -10dB
	802.11g /54Mbps : 14dBm ± 2 dB	EVM ≤ -25dB
	802.11n /MCS7 : 13dBm ± 2 dB	EVM ≤ -28dB
Spectrum Mask	Meet with IEEE standard	
Freq. Tolerance	± 15ppm	
Receive Sensitivity (11b,20MHz) @8% PER	- 11Mbps PER @ ≤ -76 dBm	-
Receive Sensitivity (11g,20MHz) @10% PER	- 54Mbps PER @ ≤ -65 dBm	-
Receive Sensitivity (11n,20MHz) @10% PER	- MCS=7 PER @ ≤ -64 dBm	-
Receive Sensitivity (11n,40MHz) @10% PER	- MCS=7, PER @ ≤ -61 dBm	-

4.2 Bluetooth Specification

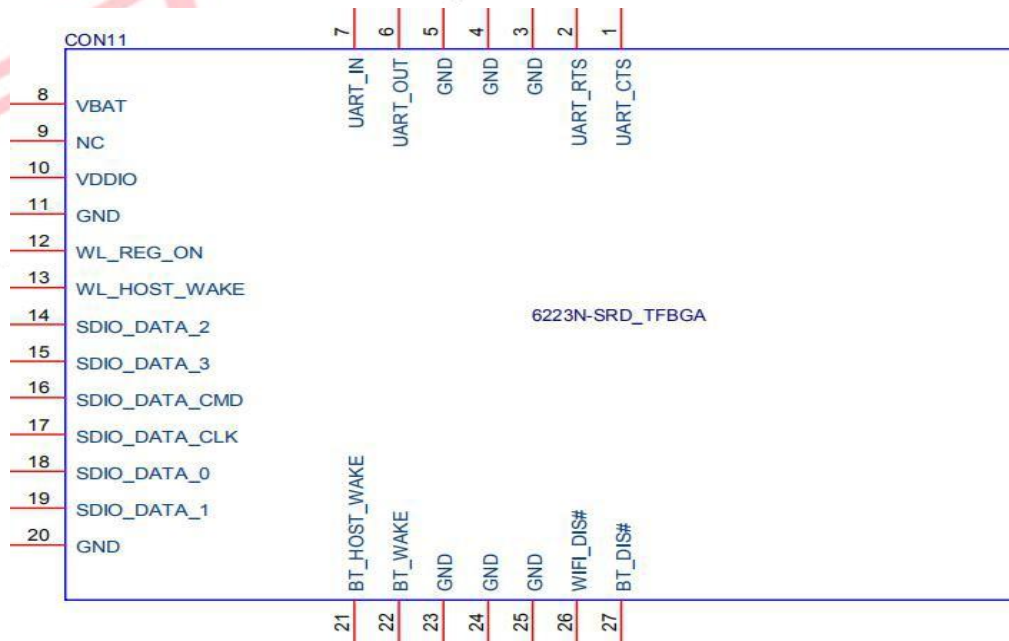
Feature	Description
General Specification	
Bluetooth Standard	Bluetooth V4.2 of 1, 2 and 3 Mbps.
Host Interface	UART
Frequency Band	2402 MHz ~ 2480 MHz
Number of Channels	79 channels
Modulation	GFSK, π/4-DQPSK, 8-DPSK
RF Specification	

	Min(dBm)	Typical(dBm)	Max(dBm)
Output Power (Class 1.5)	3	6	9
Output Power (Class 2)		2	
Sensitivity @ BER=0.1% for GFSK (1Mbps)		-86	
Sensitivity @ BER=0.01% for $\pi/4$ -DQPSK (2Mbps)		-86	
Sensitivity @ BER=0.01% for 8DPSK (3Mbps)		-80	
Maximum Input Level	GFSK (1Mbps):-20dBm		
	$\pi/4$ -DQPSK (2Mbps) :-20dBm		
	8DPSK (3Mbps) :-20dBm		
Sensitive @PER=30.8% FOR BLE		-90	

5. Pin Definition

5.1 Pin Outline

< TOP VIEW >



5.2 Pin Definition details

NO.	Name	Type	Description	Voltage
1	UART-CTS		UART-CTS	VDDIO
2	UART-RTS		UART-RTS	VDDIO
3	GND		Ground connections	
4	GND		Ground connections	
5	GND		Ground connections	
6	UART-OUT	O	UART output	VDDIO
7	UART-IN	I	UART input	VDDIO
8	VBAT	P	Supply 3.3V	3.3V
9	NC		Floating (Don't connected to	
10	VDDIO	P	I/O Voltage supply input 1.8V to 3.3V	1.8V ~ 3.3V
11	GND		Ground connections	
12	CHIP_EN	I	This pin may not supported, please NC.	3.3V
13	WL_WAKE_HOST	I/O	WLAN device wake-up host	VDDIO
14	SD_D2	I/O	SDIO Data line 2	VDDIO
15	SD_D3	I/O	SDIO Data line 3	VDDIO
16	SD_CMD	I/O	SDIO Command Input	VDDIO
17	SD_CLK	I	SDIO Clock Input	VDDIO
18	SD_D0	I/O	SDIO Data line 0	VDDIO
19	SD_D1	I/O	SDIO Data line 1	VDDIO
20	GND		Ground connections	
21	BT_HOST_WAKE		BT host wake-up device	VDDIO
22	BT_WAKE_HOST		BT device wake-up host	VDDIO
23	GND		Ground connections	
24	GND		Ground connections	
25	GND		Ground connections	
26	WIFI_DIS#		Pull high: ON (default) , Pull low: OFF External pull low can disable WL	3.3V
27	BT_DIS#		Pull high: ON (default) , Pull low: OFF External pull low can disable BT	3.3V

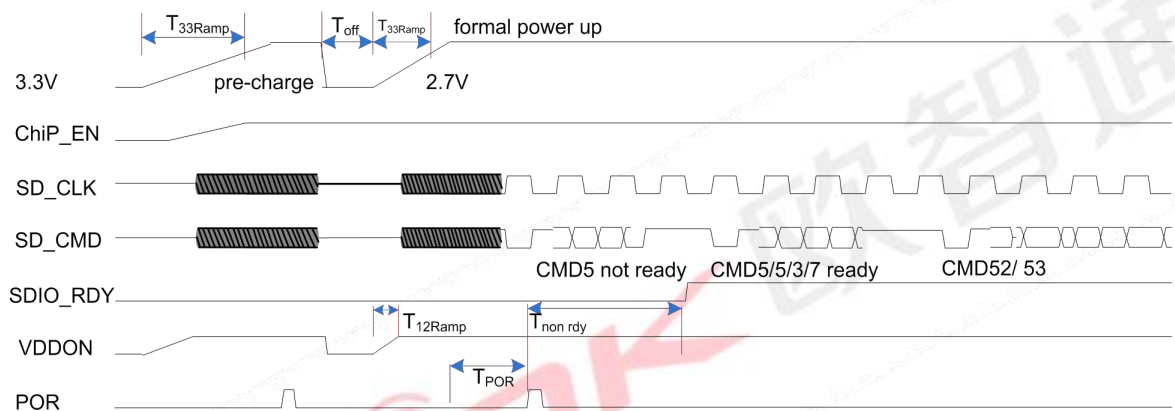
P:POWER I:INPUT O:OUTPUT

6. Electrical Specifications

6.1 Power Supply DC Characteristics

	MIN	TYP	MAX	Unit
Operating Temperature	0	25	70	deg.C
VCC33	3.0	3.3	3.6	V
VDDIO	1.62	1.8 or 3.3	3.6	V

6.2 SDIO Power-on sequence



Symbol	Min	Typical	Max	Unit
T_{33ramp}	0.2	-	No Limit	ms
T_{off}	250	500	1000	ms
T_{33ramp}	0.2	0.5	2.5	ms
T_{12ramp}	0.1	0.5	1.5	ms
T_{POR}	2	2	8	ms
$T_{non\ rdy}$	1	2	10	ms

6.3 Interface Circuit time series

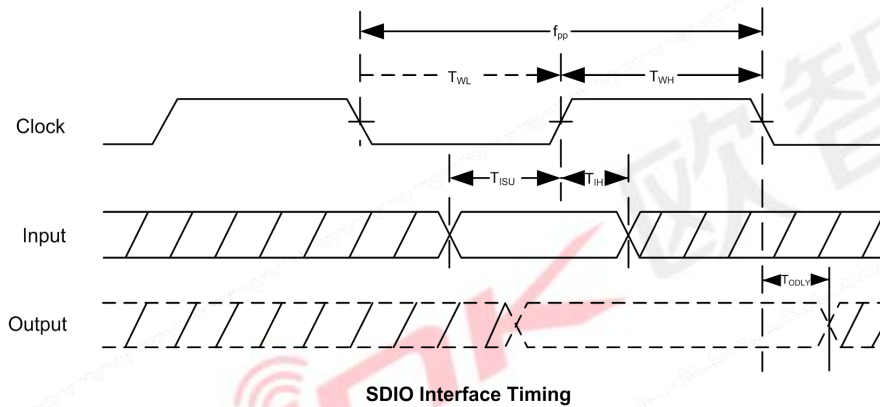
6.3.1 SDIO Pin Description

The module supports SDIO version 2.0 for all 1.8V 4-bit UHSI speeds: SDR12(25 Mbps), and SDR25(50Mbps) in addition to the 3.3V default speed(25MHz) and high speed (50 MHz). It has the ability to stop the SDIO clock and map the interrupt signal into a GPIO pin. This ‘out-of-band’ interrupt signal notifies the host when the WLAN device wants to turn on the SDIO interface. The ability to force the control of the gated clocks from within the WLAN chip is also provided.

SDIO Pin Description

SD 4-Bit Mode	
DATA0	Data Line 0
DATA1	Data Line 1 or Interrupt
DATA2	Data Line 2 or Read Wait
DATA3	Data Line 3
CLK	Clock
CMD	Command Line

6.3.2 SDIO Default Mode Timing Diagram

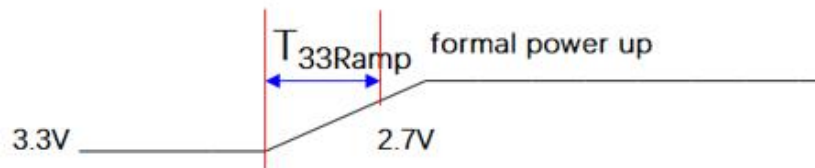


SDIO Interface Timing Parameters

NO	Parameter	Mode	MIN	MAX	Unit
f_{pp}	Clock Frequency	Default	0	25	MHz
		HS	0	50	MHz
T_{WL}	Clock Low Time	DEF	10	-	ns
		HS	7	-	ns
T_{WH}	Clock High Time	DEF	10	-	ns
		HS	7	-	ns
T_{ISU}	Input Setup Time	DEF	5	-	ns
		HS	6	-	ns
T_{IH}	Input Hold Time	DEF	5	-	ns
		HS	2	-	ns
T_{ODLY}	Output Delay Time	DEF	-	14	ns
		HS	-	14	ns

6.3.3 module power-on&off time sequence

	Min	Typical	Max	Unit
T33 power on ramp	0.2	0.5	2.5	ms
T33 power off ramp	0.2	5	10	ms



1.上下电时序请满足表格要求；

The power up ramp and power down ramp must meet the following table.

2.上下电过程如有较长时间中间电压停留都会有几率导致 efuse 被窜写；

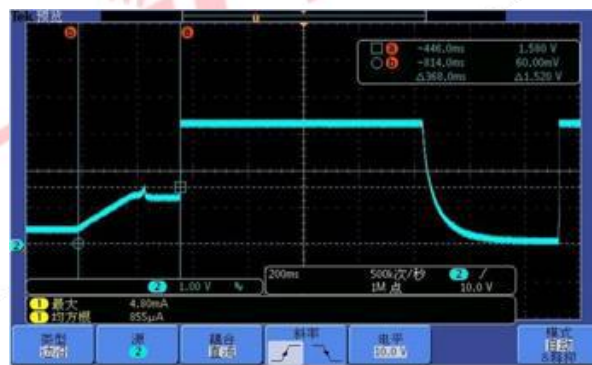
If climbing process for a long time during power-on and power-off , It may cause efuse to be overwritten.

3.建议主芯片上电完成后，再给模组上电；

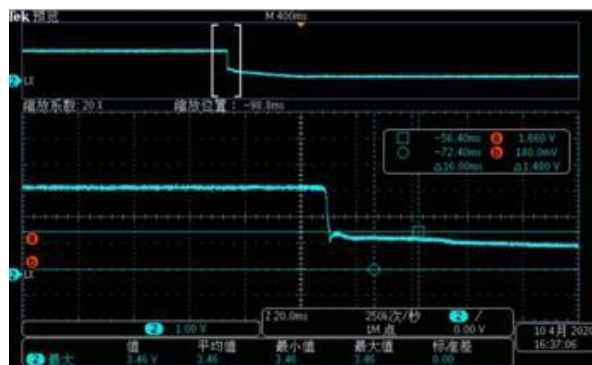
it is recommended to power on the module after platform side.

4.如有下图所示异常上下电时序，务必做相应调整符合时序规格；

If power on/off timing as below shown, must modify to meet the timing specification.



异常上电时序



异常下电时序

6.3.4 UART Interface Characteristics

The RTL8723DS UART interface is a standard 4-wire interface with RX, TX, CTS and RTS. The interface supports the Bluetooth 2.0 UART HCI H4 and H5 specifications. The default baud rate is 115.2K baud. In order to support high and low speed baud rate, the RTL8723DS provides multiple UART clocks.

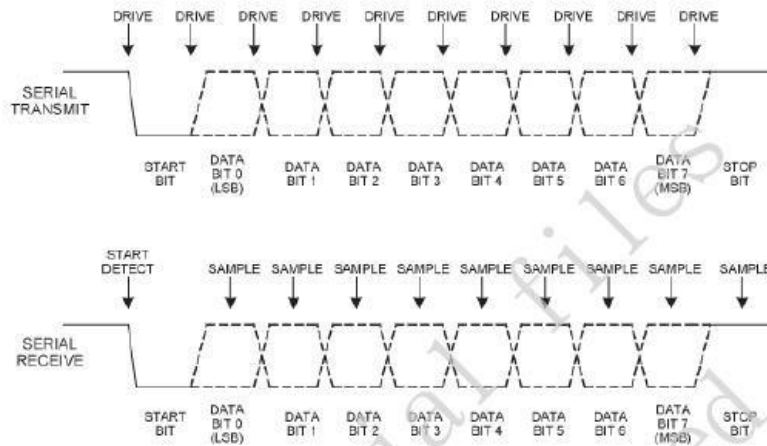


Figure 7. UART Interface Waveform

6.3.5 UART Interface Power-on Sequence

UART Hardware Flow Control Not Supported

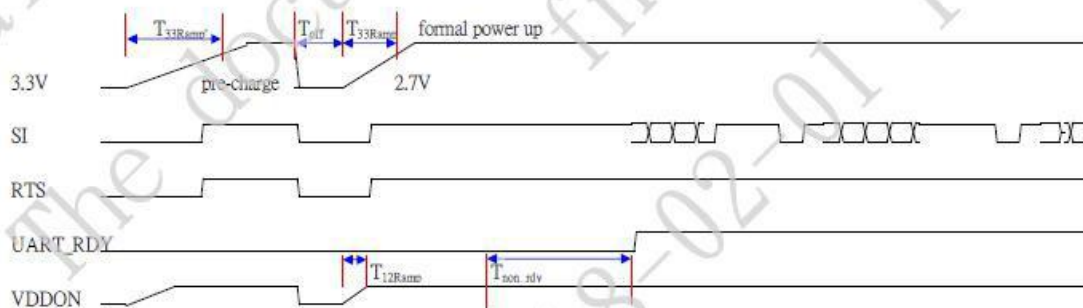
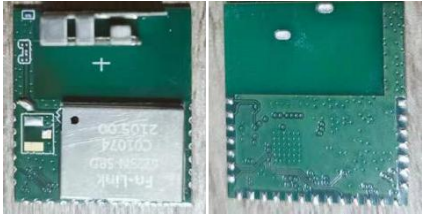
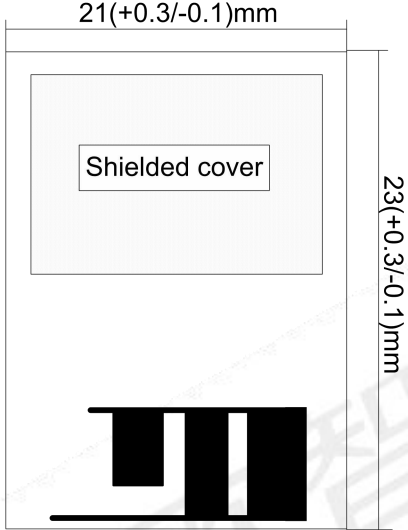
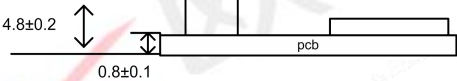


Figure 8. UART Power-On Sequence With Hardware Flow Control

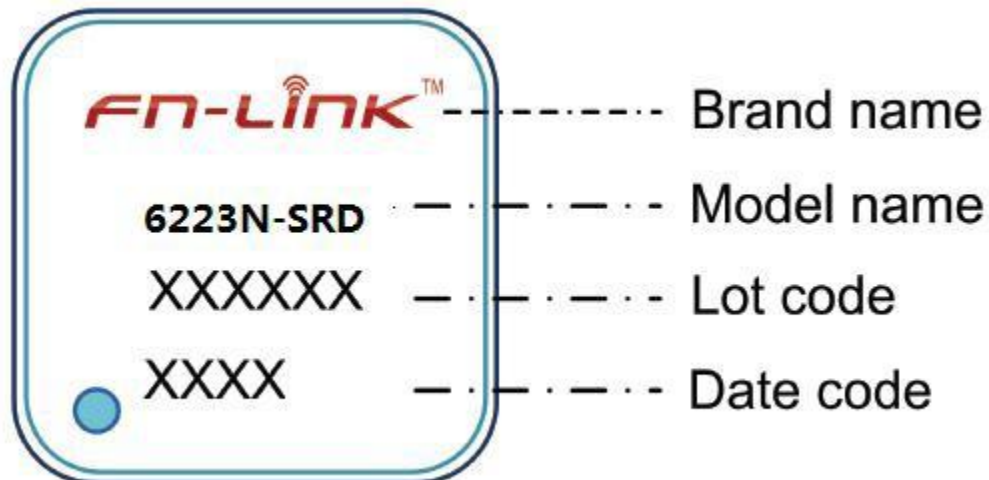
7. Size reference

7.1 Module Picture

<p>L x W : 23 x 21 (+0.3/-0.1) mm</p> 	
<p>H: 4.8 (±0.2) mm</p>	
<p>Weight</p>	<p>1.65g</p>

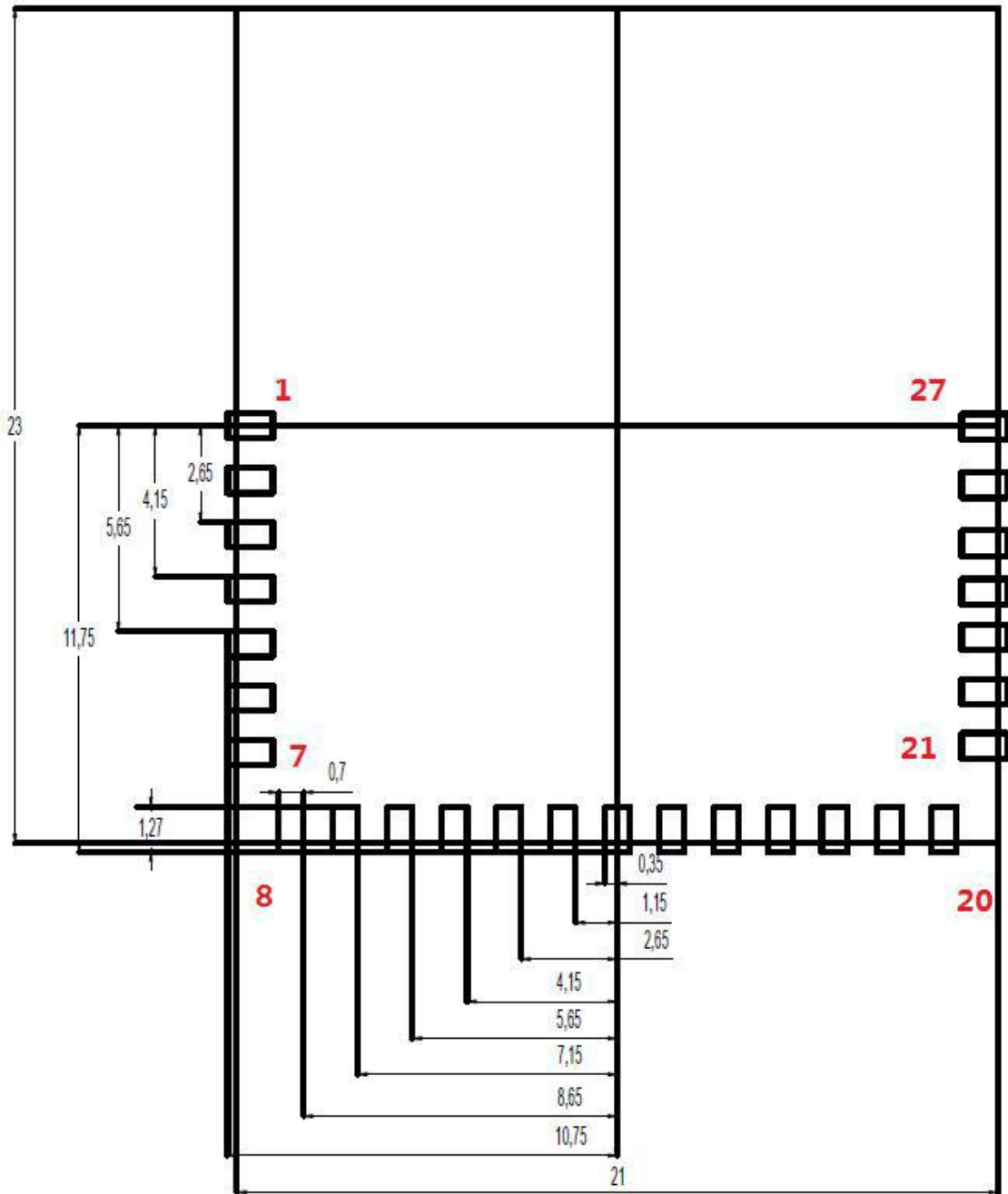
7.2 Marking Description

< TOP VIEW >

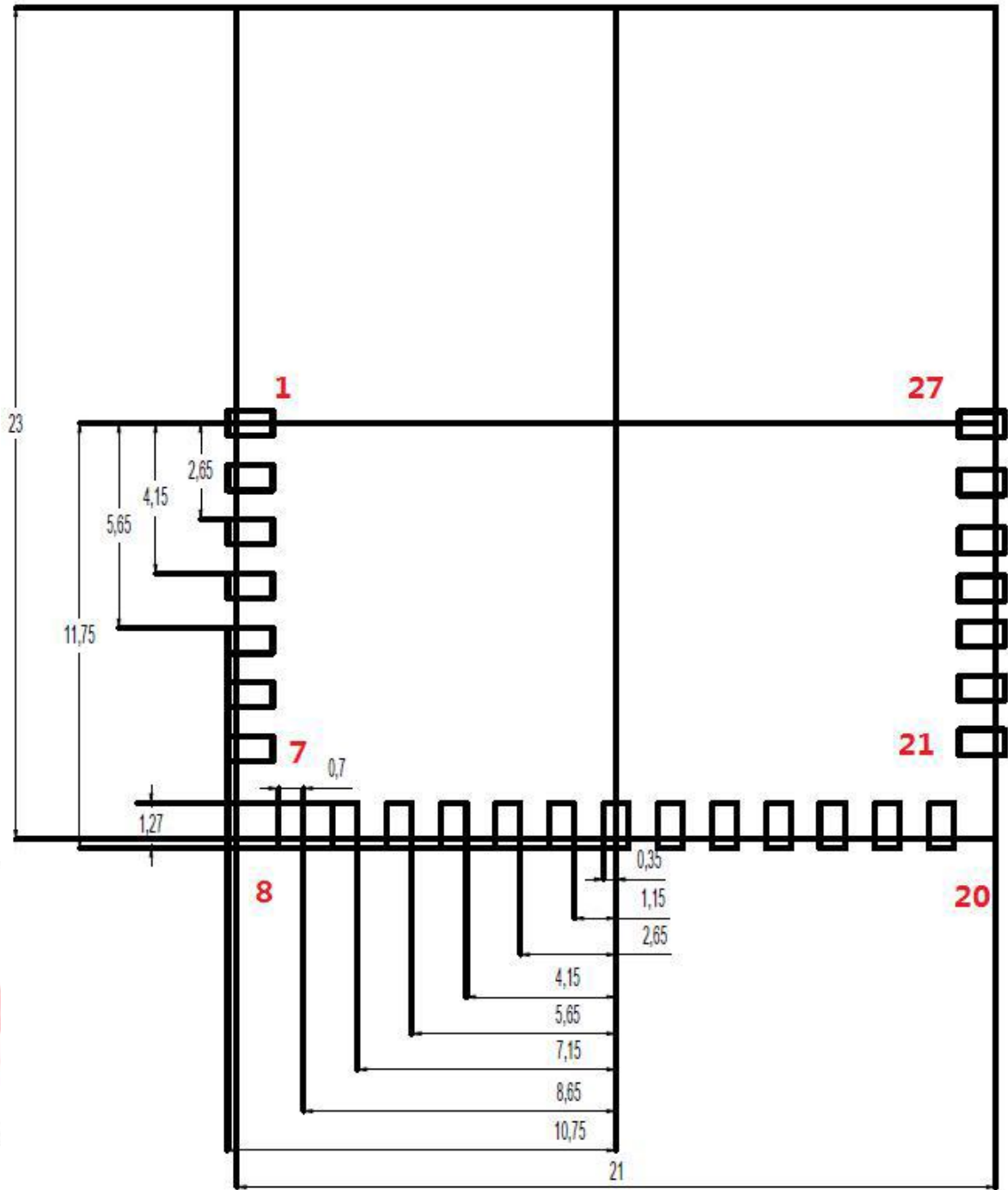


7.3 Physical Dimensions

<TOP View>



7.4 Layout Recommendation

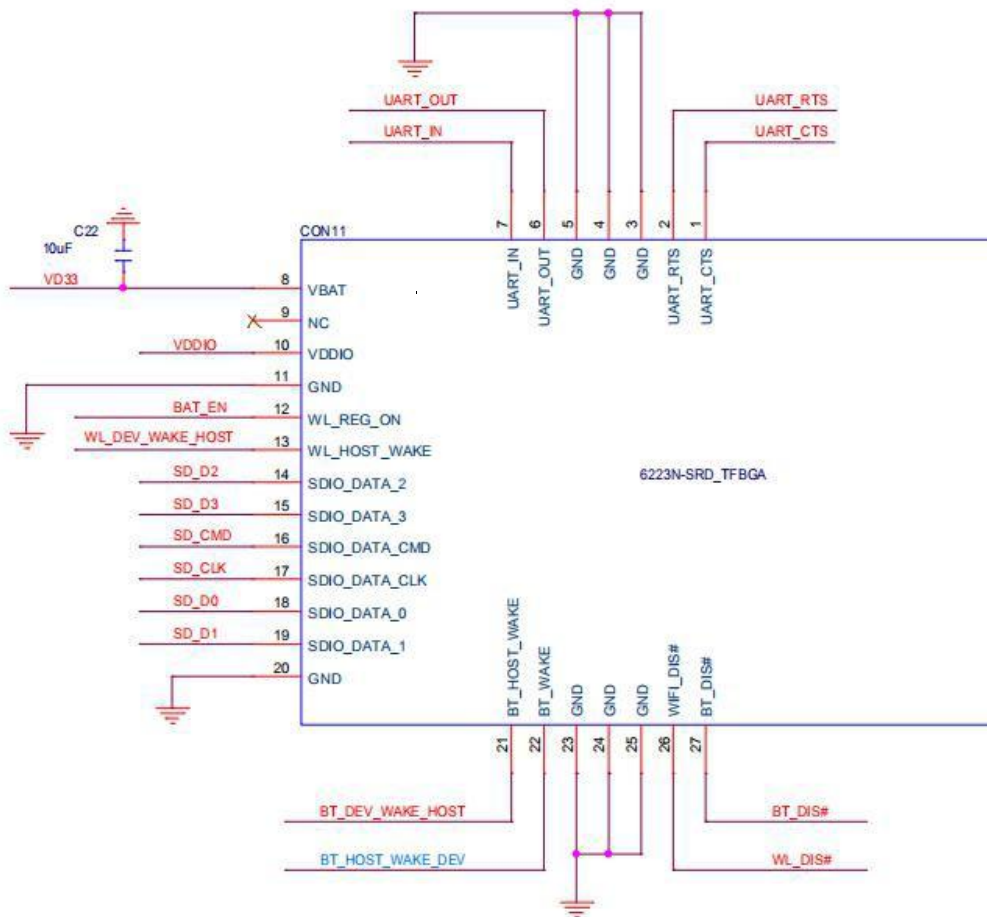


8. The Key Material List

Item	Part Name	Description	Manufacturer
1	PCB	6223N-SRD,FR4,green	XY-PCB, GDKX, Sunlord, SLPCB
2	Crystal	3225 24MHZ CL=12pF, ±10ppm	ECEC, Hosonic, TKD, JWT, TXC
3	Chipset	RTL8723DS-CG	RTL
4	Shielding	6223NSRD Shielding	信太, 精力通
5	TVS	0201 5V 0.05pF 15KV	Murata, Sunlord, 维安

9. Reference Design

9.1 Reference Design

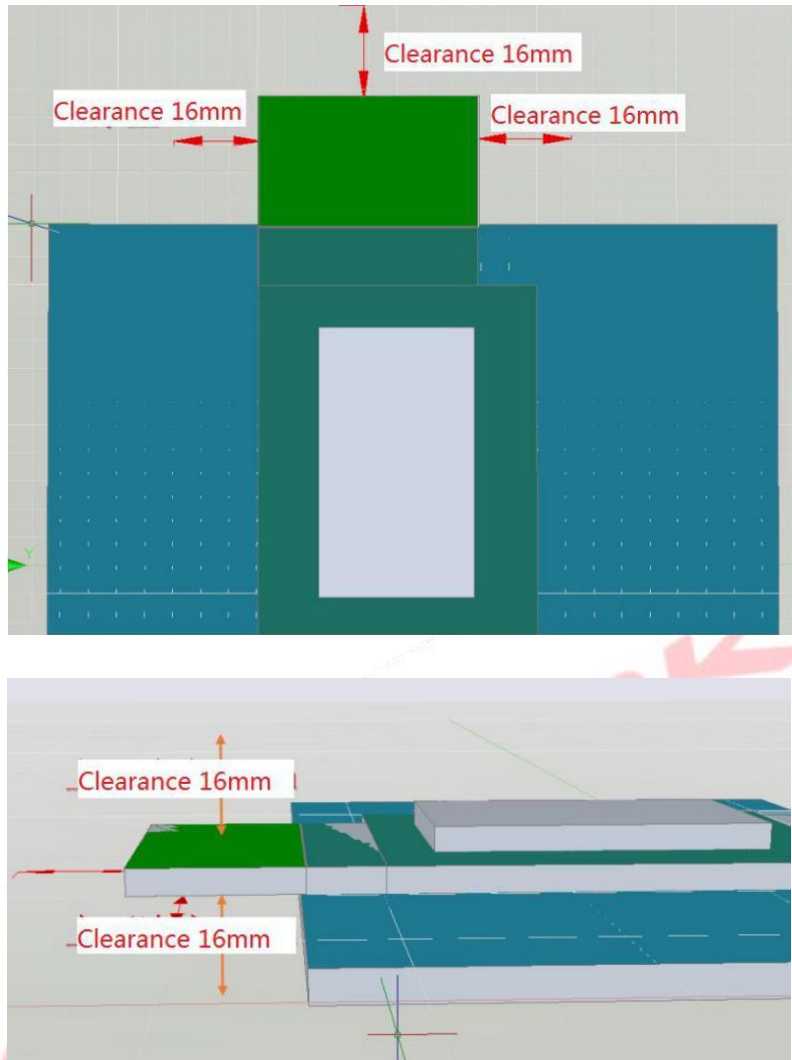


Note:

1. BAT_EN could not use for module power off, please switch the 3.3V power for module on/off.
2. please keep the antenna on no metal area.

9.2 Antenna clearance area requirements

When using PCB antenna on Wi-Fi module, make sure the distance between PCB on motherboard and other metal devices is at least 16mm. The shaded areas in the figure below need to be marked away from metal devices, sensors, interference sources, and other materials that may interfere with the signal.



Note:

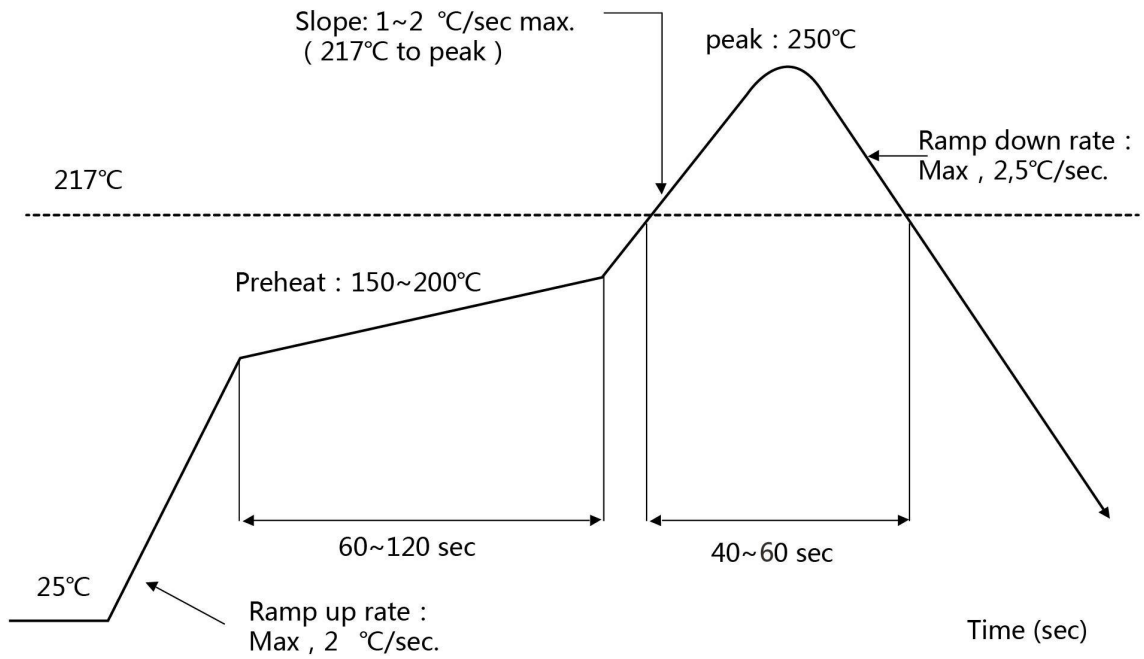
1. Fatness of module 6223N-SRD $\leq 0.1\text{mm}$
2. Please press 1 : 1 and then expand outward proportion to 0.7 mm, 0.12 mm thickness When open a stencil.
3. Take and use the WIFI/BT module, please insure the electrostatic protective measures.

10. Recommended Reflow Profile

Referred to IPC/JEDEC standard.

Peak Temperature : <250°C

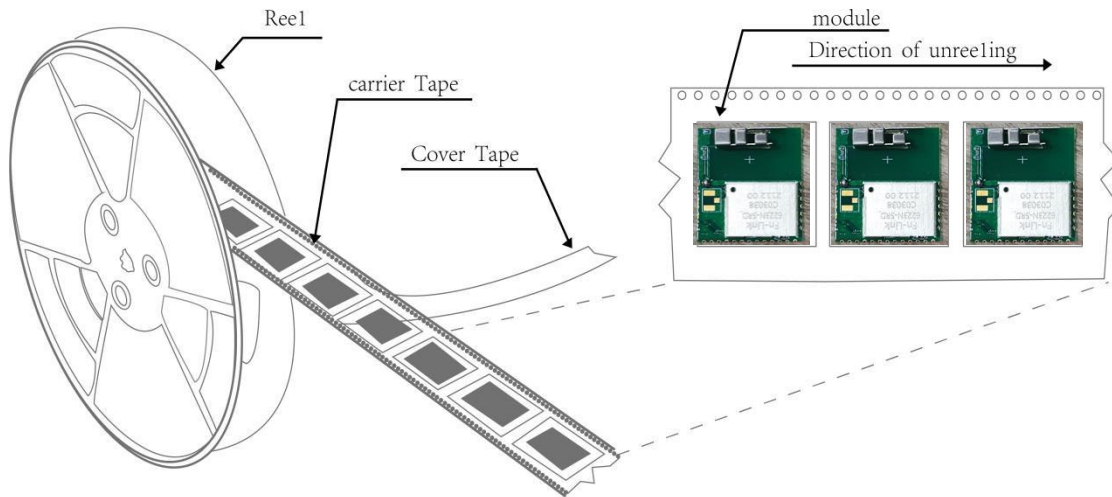
Number of Times : ≤2 times



11. Package

11.1 Reel

A roll of 350pcs



11.2 Packaging Detail

the take-up package



Using self-adhesive tape
Color of plastic disc: blue



NY bag size:TBD



size : TBD



The packing case size:TBD

12. Moisture sensitivity

The Modules is a Moisture Sensitive Device level 3, in according with standard IPC/JEDEC J-STD-020, take care

all the relatives requirements for using this kind of components.

Moreover, the customer has to take care of the following conditions:

- a) Calculated shelf life in sealed bag: 12 months at <40°C and <90% relative humidity (RH)
- b) Environmental condition during the production: 30°C / 60% RH according to IPC/JEDEC J-STD-033A paragraph 5
- c) The maximum time between the opening of the sealed bag and the reflow process must be 168 hours if condition
- b) “IPC/JEDEC J-STD-033A paragraph 5.2” is respected
- d) Baking is required if conditions b) or c) are not respected
- e) Baking is required if the humidity indicator inside the bag indicates 10% RH or more