FN-LINK欧智通

PRODUCT SPECIFICATION

H132A-S

Wi-Fi Single-band 1x1 802.11b/g/n

SDIO/UART Module Datasheet

Version:v1.6

H132A-S Module Datasheet

Ordering Information	Part NO.	Description
	FGH132ASXX-01	SV32WB01L, b/g/n Wi-Fi, 1T1R, 12X12mm, SDIO/UART, PCB V1.0,with shielding.4bit mode

Customer: _____

Customer P/N: _____

Signature: _____

Date: _____

Office: 14th floor, Block B, phoenix zhigu, Xixiang Street, Baoan District, Shenzhen

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Revision History

Version	Date	Revision Change	Draft	Checked	Approved
V1.0	2021/3/10	New version	Lxy	Lxy	Szs
V1.1	2021/06/04	增加 34 脚用途描述	Lxy	Lxy	Szs
V1.2	2021/10/14	Update module photo	LXY	LXY	QJP
V1.3	2021/10/15	Update tolerance to +/-1.5	LXY	LXY	QJP
V1.4	2022/03/04	Update IO power level	LXY	LXY	QJP
V1.5	2022/03/22	Update reference circuit	LXY	LXY	QJP
V1.6	2022/03/26	Update the specification format Change RF power tolerance to ±2dBm	Fc	LXY	QJP

1. General Description

1.1 Introduction

H132A-S is a highly integrated 2.4 GHz Wi-Fi module that support the IEEE 802.11b/g/n standard with 20/40 MHz bandwidth.

Module chipset integrates a Andes D10F 32-bit RISC core which runs at up to 480MHz , includes up to 512KB of embedded SRAM, Internal flash up to 2MB, and various peripheral interfaces, including the SPI, UART, I2C, PWM, GPIO, and multi-channel ADC. In addition, it provides SDIO2.0 slave interfaces, with clock frequency up to 50 MHz.

1.2 Description

Model Name	H132A-S
Product Description	Support Wi-Fi functionalities
Dimension	L x W x H: 12 x 12 x2.3 (typical) mm
Wi-Fi Interface	Support SDIO
OS supported	Android /Linux/ Win CE /iOS /XP/WIN7/WIN10
Operating temperature	-10°C to 85°C
Storage temperature	-40°C to 85°C

2. Features

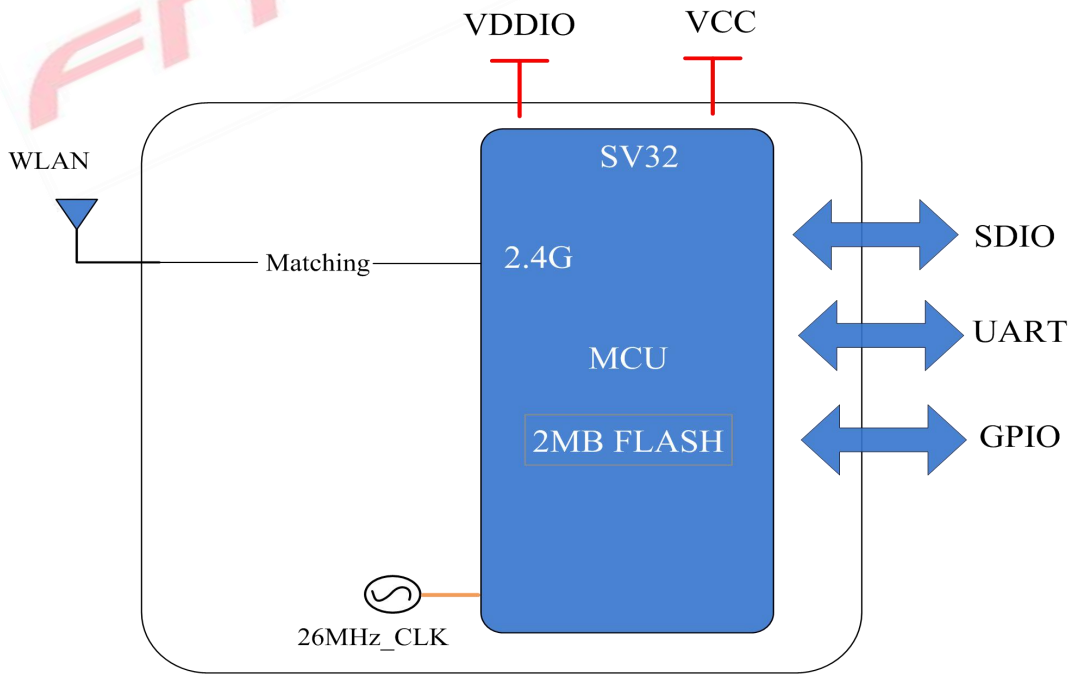
General Features

- Operate at ISM frequency bands (2.4GHz)
- Maximum rate of 150 Mbit/s@HT40 MCS7
- Low power dissipation
- PHY supporting IEEE 802.11b/g/n
- MAC supporting IEEE802.11 d/e/h/i/k/r/w
- Module integrated 32K clock
- WEP/WPA/WPA2/WPA3 /WMM for Wi-Fi
- Built-in 512 KB SRAM and 128 KB ROM
- Internal flash 2MB
- SDIO 4Line mode

WLAN Interface

- SDIO interface for Wi-Fi
- Support SDIO/UART/PWM/GPIO/I2C/ADC interface

3. Block Diagram



4. General Specification

4.1 WI-FI Specification

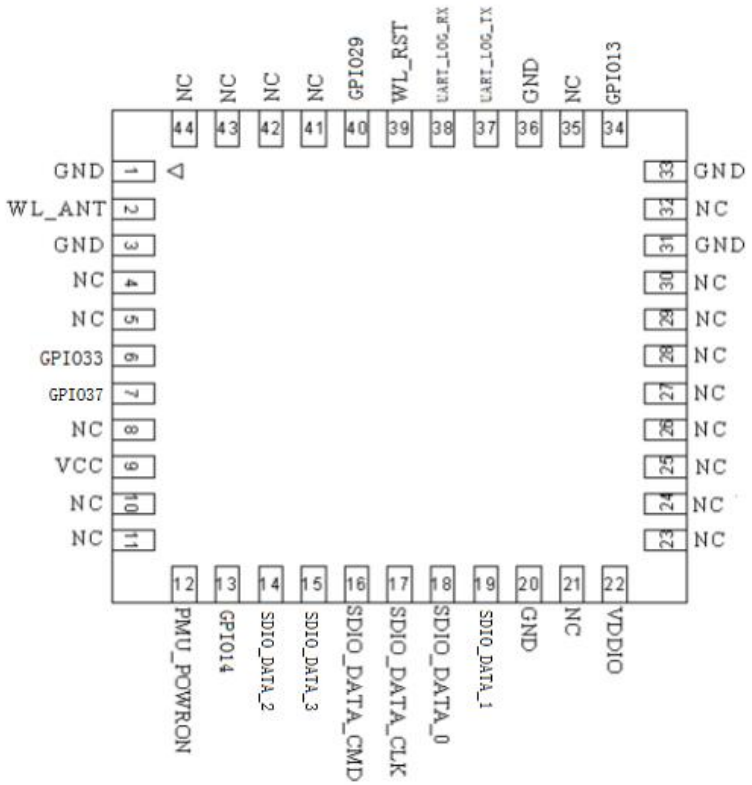
Feature	**Description**	
WLAN Standard	IEEE 802.11 b/g/n Wi-Fi compliant	
Frequency Range	2.400 GHz ~ 2.4835 GHz (2.4 GHz ISM Band)	
Number of Channels	2.4GHz：Ch1 ~ Ch14	
Test Items	**Typical Value**	**EVM**
Output Power	802.11b /11Mbps : 17dBm ± 2 dB	EVM ≤ -10dB
	802.11g /54Mbps : 15dBm ± 2 dB	EVM ≤ -25dB
	802.11n /MCS7 : 15dBm ± 2 dB	EVM ≤ -28dB
Spectrum Mask	Meet with IEEE standard	
Freq. Tolerance	±20ppm	
Test Items	**TYP Test Value**	**Standard Value**
SISO Receive Sensitivity (11b,20MHz) @8% PER	- 1Mbps PER @ -95 dBm	≤-94 dBm
	- 2Mbps PER @ -93 dBm	≤-92 dBm
	- 5.5Mbps PER @ -90 dBm	≤-89 dBm
	- 11Mbps PER @ -88 dBm	≤-87 dBm
SISO Receive Sensitivity (11g,20MHz) @10% PER	- 6Mbps PER @ -90 dBm	≤-86 dBm
	- 9Mbps PER @ -88 dBm	≤-85 dBm
	- 12Mbps PER @ -87 dBm	≤-84 dBm
	- 18Mbps PER @ -84 dBm	≤-82 dBm
	- 24Mbps PER @ -81 dBm	≤-80 dBm
	- 36Mbps PER @ -78 dBm	≤-76 dBm
	- 48Mbps PER @ -75 dBm	≤-73 dBm
	- 54Mbps PER @ -73 dBm	≤-70 dBm
SISO Receive Sensitivity (11n,20MHz) @10% PER	- MCS=0 PER @ -90 dBm	≤-86 dBm
	- MCS=1 PER @ -87 dBm	≤-83 dBm
	- MCS=2 PER @ -85 dBm	≤-81 dBm
	- MCS=3 PER @ -82 dBm	≤-79 dBm
	- MCS=4 PER @ -79 dBm	≤-76 dBm
	- MCS=5 PER @ -74 dBm	≤-73 dBm
	- MCS=6 PER @ -73 dBm	≤-71 dBm
	- MCS=7 PER @ -71 dBm	≤-69 dBm
SISO Receive Sensitivity (11n,40MHz) @10% PER	- MCS=0 PER @ -87 dBm	≤-83 dBm
	- MCS=1 PER @ -84 dBm	≤-80 dBm

	- MCS=2	PER @ -82 dBm	≤-79 dBm
	- MCS=3	PER @ -79 dBm	≤-76 dBm
	- MCS=4	PER @ -76 dBm	≤-73 dBm
	- MCS=5	PER @ -71 dBm	≤-70 dBm
	- MCS=6	PER @ -70 dBm	≤-68 dBm
	- MCS=7	PER @ -68 dBm	≤-66 dBm
Maximum Input Level	802.11b : -10 dBm		
	802.11g/n : -20 dBm		
Antenna Reference	PCB antenna with 0~2 dBi peak gain		

5. Pin Definition

5.1 Pin Outline

< TOP VIEW >



5.2 Pin Definition details

NO	Name	Type	Description	Voltage
1	GND	—	Ground connections	
2	WL_ANT	I/O	RF I/O port	
3	GND	—	Ground connections	
4	NC	—	Floating (Don't connected to ground)	
5	NC	—	Floating (Don't connected to ground)	
6	GPIO33	I/O	Muti funtion I/O	VDDIO
7	GPIO37	I/O	Muti funtion I/O	VDDIO
8	NC	—	Floating (Don't connected to ground)	
9	VCC	P	Main power voltage source input 3.13V-3.46V	3.3V
10	NC	—	Floating (Don't connected to ground)	
11	NC	—	Floating (Don't connected to ground)	
12	PMU_POWRON	I	Enable pin for WLAN device Defualt ON: pull high ; OFF: pull low	VCC
13	GPIO14	I/O	Muti funtion I/O	VDDIO
14	SDIO_DATA_2	I/O	SDIO data line 2, GPIO17	VDDIO
15	SDIO_DATA_3	I/O	SDIO data line 3, GPIO18	VDDIO
16	SDIO_DATA_CMD	I/O	SDIO command line, GPIO19	VDDIO
17	SDIO_DATA_CLK	I	SDIO clock line, GPIO20	VDDIO
18	SDIO_DATA_0	I/O	SDIO data line 0, GPIO21	VDDIO
19	SDIO_DATA_1	I/O	SDIO data line 1, GPIO22	VDDIO
20	GND	—	Ground connections	
21	NC	—	Floating (Don't connected to ground)	
22	VDDIO	P	I/O Voltage supply input typ= 3.3V	VDDIO
23	NC	—	Floating (Don't connected to ground)	
24	NC	—	Floating (Don't connected to ground)	
25	NC	—	Floating (Don't connected to ground)	
26	NC	—	Floating (Don't connected to ground)	
27	NC	—	Floating (Don't connected to ground)	
28	NC	—	Floating (Don't connected to ground)	
29	NC	—	Floating (Don't connected to ground)	
30	NC	—	Floating (Don't connected to ground)	
31	GND	—	Ground connections	
32	NC	—	Floating (Don't connected to ground)	
33	GND	—	Ground connections	

34	GPIO13	I/O	Muti funtion I/O H: to download mode;L:to normal mode Don't pull high, better10K pull low this pin.	VCC
35	NC	—	Floating (Don't connected to ground)	
36	GND	—	Ground connections	
37	UART_LOG_TX	—	UART0_LOG_TX,GPIO01 For firmware download,debug	VCC
38	UART_LOG_RX	—	UART0_LOG_RX,GPIO00 For firmware download,debug	VCC
39	WL_RST	I/O	Wi-Fi reset pin. GPIO36 Muti funciton I/O	VDDIO
40	GPIO29	I/O	Muti funtion I/O	VDDIO
41	NC	—	Floating (Don't connected to ground)	
42	NC	—	Floating (Don't connected to ground)	
43	NC	—	Floating (Don't connected to ground)	
44	NC	—	Floating (Don't connected to ground)	

P:POWER I:INPUT O:OUTPUT

5.3 Muti Pin definition

GPIO pin can configure as muti function,detail see below information.

Name	Boot Strapping ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
GPIO00	AICE_TMSC	ADC0	BT_SW	UART0_RXD				GPIO00
GPIO01	AICE_TCKC	ADC1	WIFI_TX_SW	UART0_TXD				GPIO01
GPIO13	GPIO13							GPIO13
GPIO14	GPIO14			PDMTX0_DOUT0				GPIO14
GPIO17	GPIO17	SD_DATA2	UART2_NCTS					GPIO17
GPIO18	GPIO18	SD_DATA3		DATASPISLAVE_CSN	SPISLV1_CSN	SPIMAS1_CSN		GPIO18
GPIO19	GPIO19	SD_CMD		DATASPISLAVE_MOSI	SPISLV1_MOSI	SPIMAS1_MOSI		GPIO19
GPIO20	GPIO20	SD_CLK		DATASPISLAVE_SCLK	SPISLV1_MISO	SPIMAS1_MISO		GPIO20
GPIO21	GPIO21	SD_DATA0		DATASPISLAVE_MISO	SPISLV1_SCLK	SPIMAS1_SCLK		GPIO21
GPIO22	GPIO22	SD_DATA1	UART2_NRTS					GPIO22
GPIO29	GPIO29	ADC3			UART1_RXD			GPIO29
GPIO33	GPIO33				UART1_TXD	WIFI_TX		GPIO33
GPIO36	GPIO36	ADC6	I2C0_SCL	UART2_RXD		BT_IN_PROCESS	BT_SW	GPIO36
GPIO37	GPIO37	ADC7	I2C0_SDA	UART2_TXD		BT_PTI3	WIFI_TX_SW	GPIO37

Table 25: IOT ADC Specifications

Parameter	Description	Condition/Notes	Min	Typ.	Max	Unit
Nbits	Number of bits			12		Bits
INL	Integral nonlinearity	Histogram method over full scale		±1.5	±3	LSB
DNL	Differential nonlinearity	Histogram method over full scale		±1	±2	LSB
Input Range			0		3.3	V
Input impedance				>1M		Ohms
FCLK	Clock rate	Successive approximation input clock rate		20		MHz
Input capacitance				5		pF
Number of channels				5		
Fsample	Sampling rate of each ADC			1		MSPS
F_input_max	Maximum input signal frequency			TBD		kHZ
I_active	Active supply current	Average for ADC during conversion		<0.9		mA
I_PD	Power-down supply current for core supply	Disable ADC		TBD		uA
Absolute offset error				TBD		mV
Gain error				TBD		%

6. Electrical Specifications

6.1 Power Supply DC Characteristics

	MIN	TYP	MAX	Unit
Operating Temperature	-10	25	85	deg.C
VCC	3.13	3.3	3.46	V
VDDIO	1.75	3.3V	3.46	V

6.2 Power Consumption

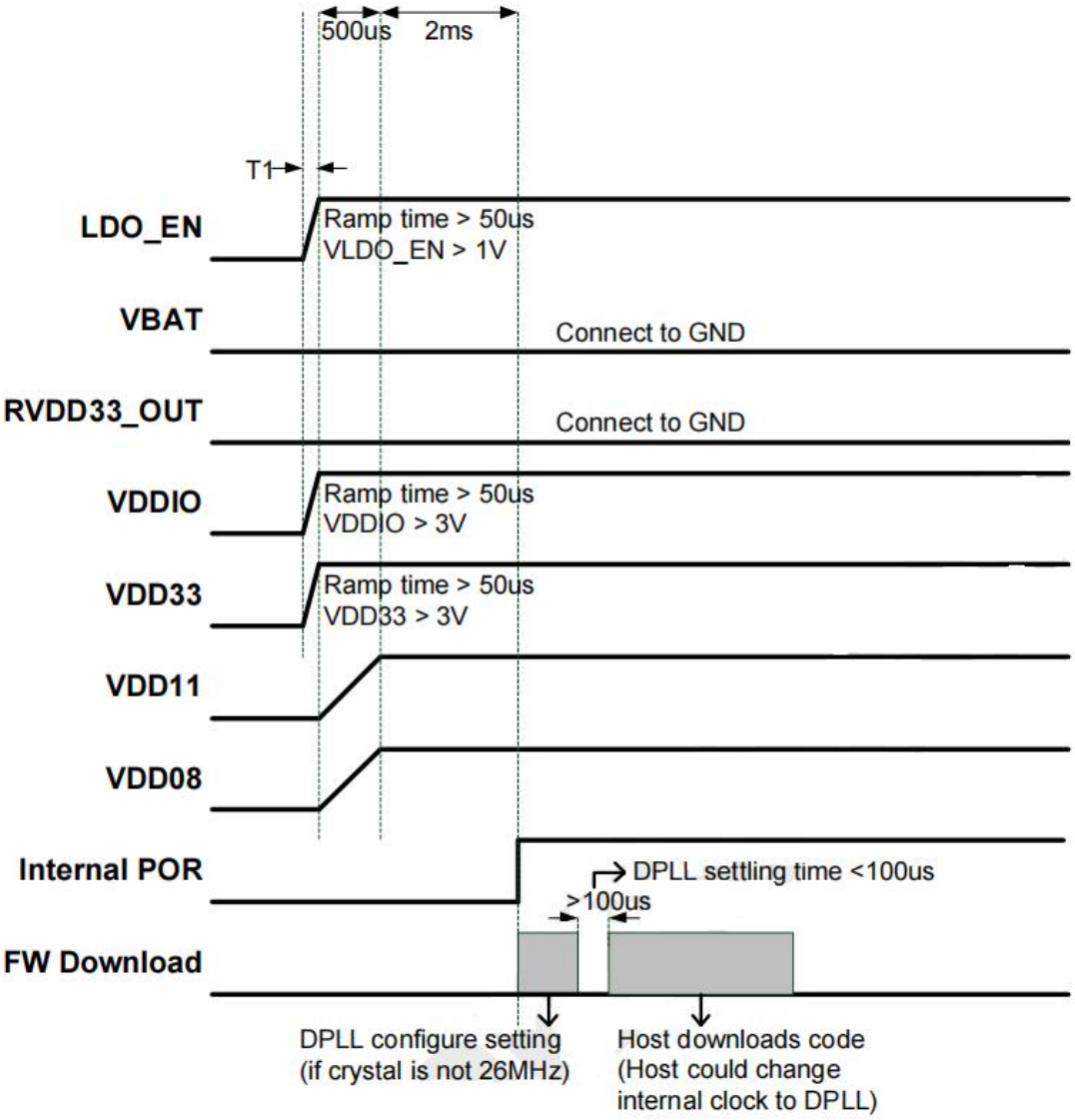
Power Consumption		VCC = 3.3V(Unit:mA)
	Power saving	0.17@DTIM3,MCU off
	TX Test mode (2.4G HT20@17dbm)	212
	RX Test mode (2.4G HT20)	47.5
	Power off	<1uA

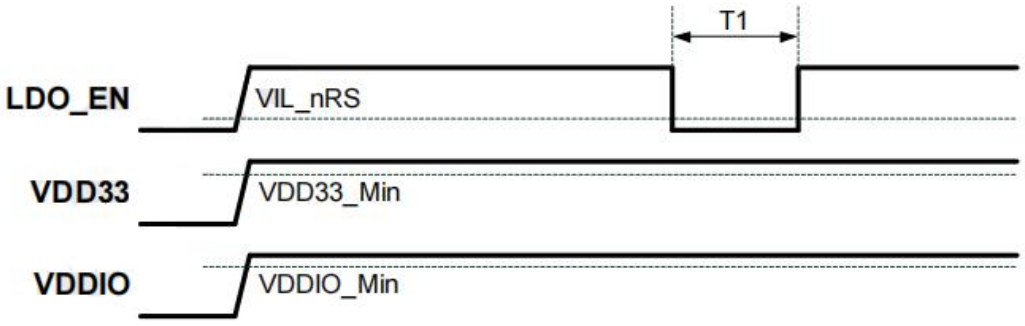
6.3 Power-on sequence

Below shows the VDD33=3.3V power-on sequence of the SV32WB0xx from power-up to firmware download, including the initial device power-on reset evoked by LDO_EN signal. The LDO_EN input level must be kept above the threshold voltage. After initial power-on, the LDO_EN signal can be held low to turn off the SV32WB0xx or pulsed low to induce a subsequent reset.

After LDO_EN is asserted, the host starts the power-on sequence of the SV32WB0xx. From that point, the typical SV32WB0xx power-on sequence is shown below:

1. Within T1+2.5ms, the internal power-on reset (POR) will be done. And host could download firmware code of DPLL setting if the crystal is not default setting, 26MHz. The internal running clock is crystal frequency.
2. After 100us of DPLL settling time, host could set internal clock to full speed and finish all the downloading of firmware code.





Reset Timing with typical power

6.4 Interface Circuit time series

6.4.1 SDIO Pin Description

The secure digital input/output (SDIO) interface supports three working modes:

Default speed mode (DS)

The maximum frequency of the interface clock is 25 MHz. The interface clock can work in 1-bit mode .

High speed mode (HS)

The maximum frequency of the interface clock is 50 MHz.

SDR25 mode

The maximum frequency of the interface clock is 50 MHz

SDIO Pin Description

SD 4-Bit Mode	
DATA0	Data Line 0
DATA1	Data Line 1
DATA2	Data Line 2
DATA3	Data Line 3
CLK	Clock
CMD	Command Line

6.4.2 SDIO CLK Timing Diagram

DS Mode

The DS mode is the default mode after the SDIO is powered on. To ensure compatibility with various host components, the DS mode requires a low working rate and supports only the 25 MHz clock.

Clock parameters in DS mode (VDDIO = 3.3 V)

Parameter	Symbol	Min.	Max.	Unit	Remarks
Clock CLK (All values are referenced to min(V_{IH}) and max(V_{IL}))					
Clock frequency Date Transfer Mode	f_{PP}	-	25	MHz	$C_{CARD} \leq 10$ pF
Clock frequency Identification Mode	f_{OD}	-	400	kHz	$C_{CARD} \leq 10$ pF
Clock low time	t_{WL}	17	-	ns	$C_{CARD} \leq 10$ pF
Clock high time	t_{WH}	17	-	ns	$C_{CARD} \leq 10$ pF
Clock rise time	t_{TLH}	-	3	ns	$C_{CARD} \leq 10$ pF
Clock fall time	t_{THL}	-	3	ns	$C_{CARD} \leq 10$ pF

Clock parameters in DS mode (VDDIO = 1.8 V)

Parameter	Symbol	Min.	Max.	Unit	Remarks
Clock CLK (All values are referenced to min(V_{IH}) and max(V_{IL}))					
Clock frequency Date Transfer Mode	f_{PP}	-	25	MHz	$C_{CARD} \leq 10$ pF
Clock frequency Identification Mode	f_{OD}	-	400	kHz	$C_{CARD} \leq 10$ pF
Clock low time	t_{WL}	14	-	ns	$C_{CARD} \leq 10$ pF
Clock high time	t_{WH}	14	-	ns	$C_{CARD} \leq 10$ pF
Clock rise time	t_{TLH}	-	6	ns	$C_{CARD} \leq 10$ pF
Clock fall time	t_{THL}	-	6	ns	$C_{CARD} \leq 10$ pF

Figure 8-6 shows the output data timing in DS mode. tISU is the setup time, that is, the stability time required by the data of the SDIO interface before clock sampling in this mode. tIH is the hold time, that is, the time required by the data of the SDIO interface to retain the original level after clock sampling in this mode.

Figure 8-6 Input timing in DS mode

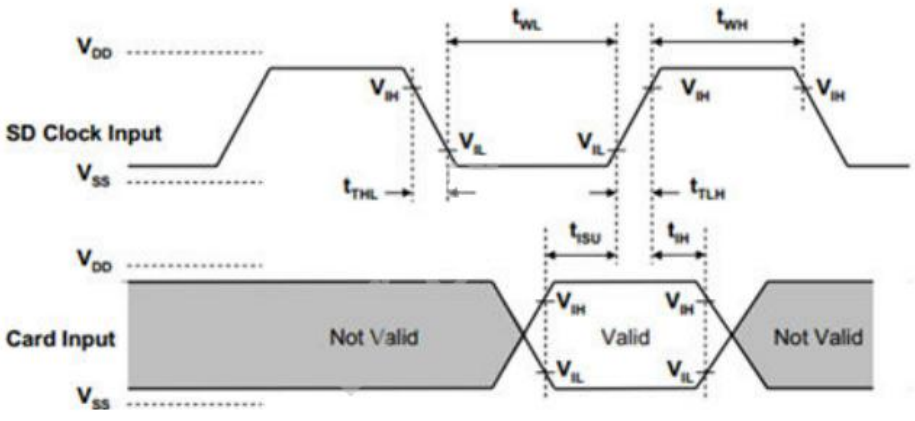


Figure 8-7 shows the input data timing in DS mode. Where, tODLY(max) is the maximum delay of the output data relative to the clock falling edge, and tODLY(min) is the minimum delay of the output data relative to the clock falling edge.

Figure 8-7 Output timing in DS mode

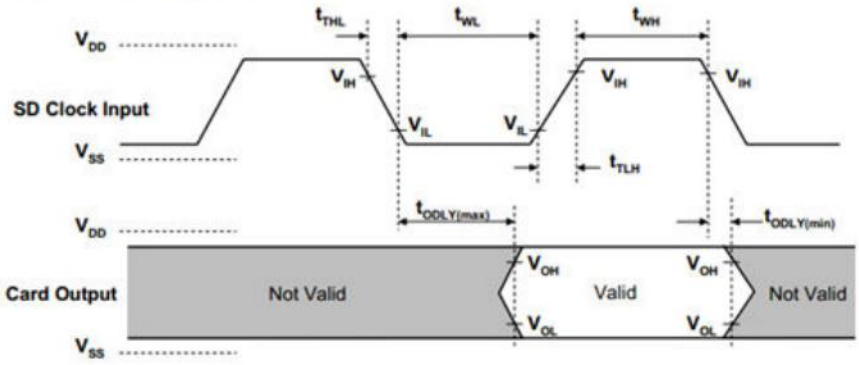


Table 8-12 describes the timing restrictions in DS mode.

Table 8-12 Timing restrictions in DS mode

Parameter	Symbol	Min.	Max.	Unit	Remarks
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	3.5	-	ns	$C_{CARD} \leq 10$ pF
Input hold time	t_{IH}	0	-	ns	$C_{CARD} \leq 10$ pF
Outputs CMD, DAT(referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}	-	11	ns	$C_L \leq 40$ pF
Output Delay time during Identification Mode	t_{ODLY}	-	11	ns	$C_L \leq 40$ pF

Note: In DS mode, the output data is referenced to the clock falling edge, and the input data is referenced to the clock rising edge.

HS Mode

The HS mode is entered after the SDIO is powered on and initialized because a higher working rate than the DS mode is required. In HS mode, the clock supports 50 MHz. For details about the restrictions on the clock, see **Table 8-13**.

Table 8-13 Clock parameters in HS mode (VDDIO = 3.3 V)

Parameter	Symbol	Min.	Max.	Unit	Remarks
Clock CLK (All values are referenced to min(V_{IH}) and max(V_{IL}))					
Clock frequency Date Transfer Mode	f_{PP}	-	50	MHz	$C_{CARD} \leq 10$ pF
Clock low time	t_{WL}	7	-	ns	$C_{CARD} \leq 10$ pF
Clock high time	t_{WH}	7	-	ns	$C_{CARD} \leq 10$ pF
Clock rise time	t_{TLH}	-	3	ns	$C_{CARD} \leq 10$ pF
Clock fall time	t_{THL}	-	3	ns	$C_{CARD} \leq 10$ pF

Table 8-14 Clock parameters in HS mode (VDDIO = 1.8 V)

Parameter	Symbol	Min.	Max.	Unit	Remarks
Clock CLK (All values are referenced to min(V_{IH}) and max(V_{IL}))					
Clock frequency Date Transfer Mode	f_{PP}	-	50	MHz	$C_{CARD} \leq 10$ pF
Clock low time	t_{WL}	4	-	ns	$C_{CARD} \leq 10$ pF
Clock high time	t_{WH}	4	-	ns	$C_{CARD} \leq 10$ pF
Clock rise time	t_{TLH}	-	6	ns	$C_{CARD} \leq 10$ pF
Clock fall time	t_{THL}	-	6	ns	$C_{CARD} \leq 10$ pF

Figure 8-8 shows the input data timing in HS mode. tISU is the setup time, that is, the stability time required by the data of the SDIO interface before clock sampling in this mode. tIH is the hold time, that is, the time required by the data of the SDIO interface to retain the original level after clock sampling in this mode

Figure 8-8 Input timing in HS mode

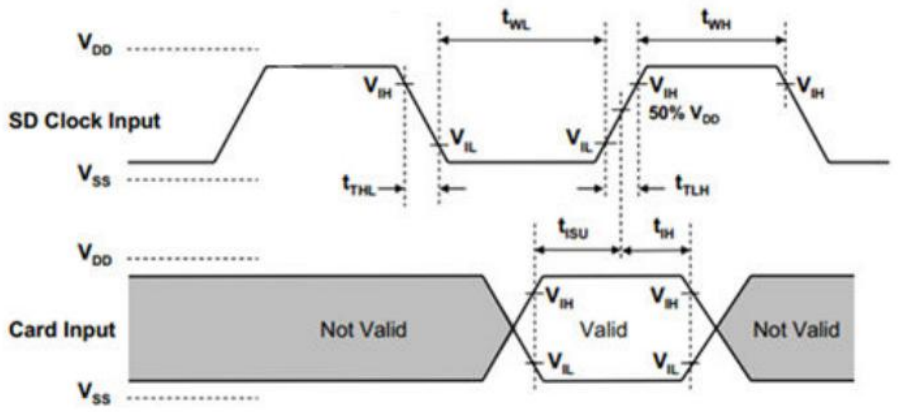


Figure 8-9 shows the input data timing in HS mode. Where, tODLY(max) is the maximum delay of the output data relative to the clock rising edge, and tOH is the minimum delay of the output data relative to the clock rising edge.

Figure 8-9 Output timing in HS mode

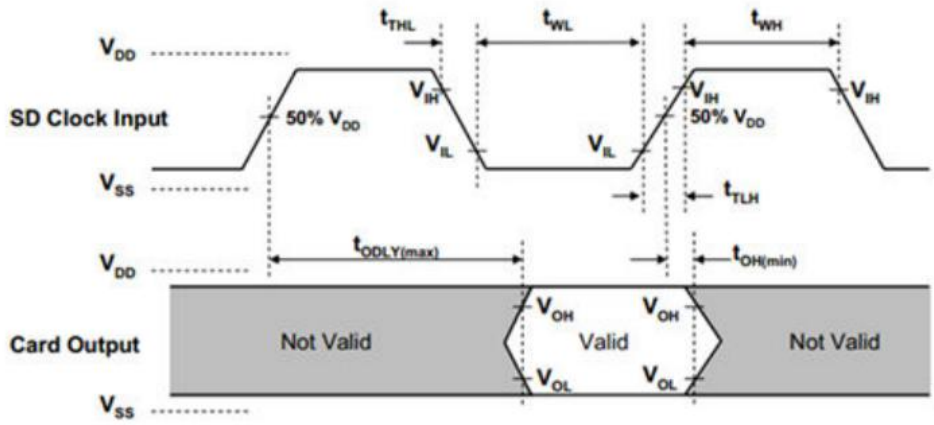


Table 8-15 describes the timing restrictions in HS mode.

Table 8-15 Timing restrictions in HS mode (VDDIO = 3.3 V)

Parameter	Symbol	Min.	Max.	Unit	Remarks
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	3.5	-	ns	$C_{CARD} \leq 10$ pF
Input hold time	t_{IH}	0	-	ns	$C_{CARD} \leq 10$ pF
Outputs CMD, DAT(referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}	-	12	ns	$C_L \leq 40$ pF
Output Hold time	t_{OH}	3	-	ns	$C_L \leq 40$ pF
Total System Capacitance for each line	C_L	-	40	pF	1 card

Table 8-16 Timing restrictions in HS mode (VDDIO = 1.8 V)

Parameter	Symbol	Min.	Max.	Unit	Remarks
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	3.5	-	ns	$C_{CARD} \leq 10$ pF
Input hold time	t_{IH}	0	-	ns	$C_{CARD} \leq 10$ pF
Outputs CMD, DAT(referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}	-	18	ns	$C_L \leq 40$ pF
Output Hold time	t_{OH}	4.5	-	ns	$C_L \leq 40$ pF
Total System Capacitance for each line	C_L	-	40	pF	1 card

Note: The data signal timing in HS mode is different from that in DS mode. The output data and input data are referenced to the clock rising edge.

SDR25 Mode

The SDR25 mode is entered only after the voltage of the SDIO is switched. In this mode, the maximum interface clock frequency is 50 MHz. **Table 8-17** describes the clock restrictions.

Table 8-17 Clock parameters in SDR25 mode (VDDIO = 3.3 V)

Parameter	Symbol	Min.	Max.	Unit	Remarks
Clock CLK (All values are referenced to min(V_{IH}) and max(V_{IL}))					
Clock frequency Date Transfer Mode	f_{PP}	-	50	MHz	$C_{CARD} \leq 10$ pF
Clock low time	t_{WL}	7	-	ns	$C_{CARD} \leq 10$ pF
Clock high time	t_{WH}	7	-	ns	$C_{CARD} \leq 10$ pF
Clock rise time	t_{TLH}	-	3	ns	$C_{CARD} \leq 10$ pF
Clock fall time	t_{THL}	-	3	ns	$C_{CARD} \leq 10$ pF

Table 8-18 Clock parameters in SDR25 mode (VDDIO = 1.8 V)

Parameter	Symbol	Min.	Max.	Unit	Remarks
Clock CLK (All values are referenced to min(V_{IH}) and max(V_{IL}))					
Clock frequency Date Transfer Mode	f_{PP}	-	50	MHz	$C_{CARD} \leq 10$ pF
Clock low time	t_{WL}	4	-	ns	$C_{CARD} \leq 10$ pF
Clock high time	t_{WH}	4	-	ns	$C_{CARD} \leq 10$ pF
Clock rise time	t_{TLH}	-	6	ns	$C_{CARD} \leq 10$ pF
Clock fall time	t_{THL}	-	6	ns	$C_{CARD} \leq 10$ pF

Table 8-19 Timing restrictions in SDR25 mode (VDDIO = 3.3 V)

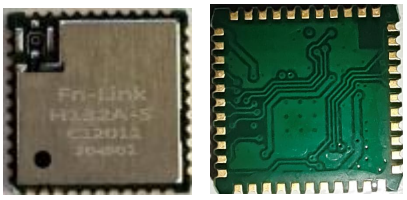
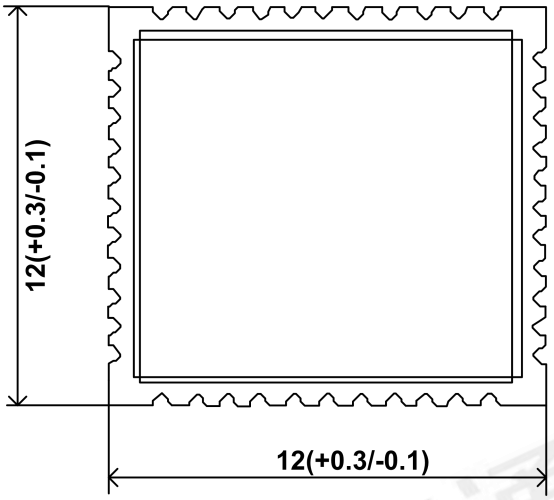
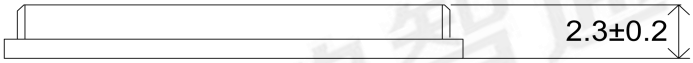
Parameter	Symbol	Min.	Max.	Unit	Remarks
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	3.5	-	ns	$C_{CARD} \leq 10$ pF
Input hold time	t_{IH}	0	-	ns	$C_{CARD} \leq 10$ pF
Outputs CMD, DAT(referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}	-	12	ns	$C_L \leq 40$ pF
Output Hold time	t_{OH}	3	-	ns	$C_L \leq 40$ pF
Total System Capacitance for each line	C_L	-	40	pF	1 card

Table 8-20 Timing restrictions in SDR25 mode (VDDIO = 1.8 V)

Parameter	Symbol	Min.	Max.	Unit	Remarks
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	3.5	-	ns	$C_{CARD} \leq 10$ pF
Input hold time	t_{IH}	0	-	ns	$C_{CARD} \leq 10$ pF
Outputs CMD, DAT(referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}	-	18	ns	$C_L \leq 40$ pF
Output Hold time	t_{OH}	4.5	-	ns	$C_L \leq 40$ pF
Total System Capacitance for each line	C_L	-	40	pF	1 card

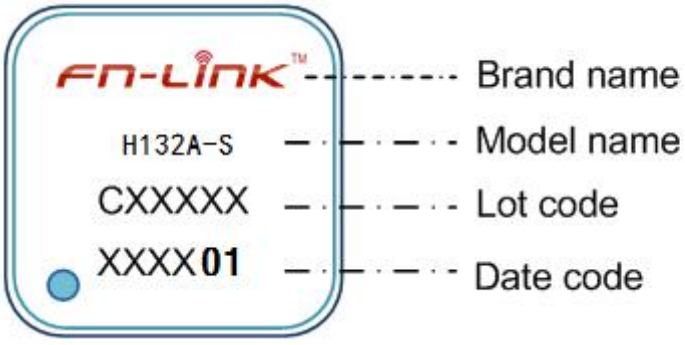
7. Size reference

7.1 Module Picture

L x W : 12 x 12 (+0.3/-0.1) mm 	
H: 2.3 (±0.2) mm	
Weight	0.66g

7.2 Marking Description

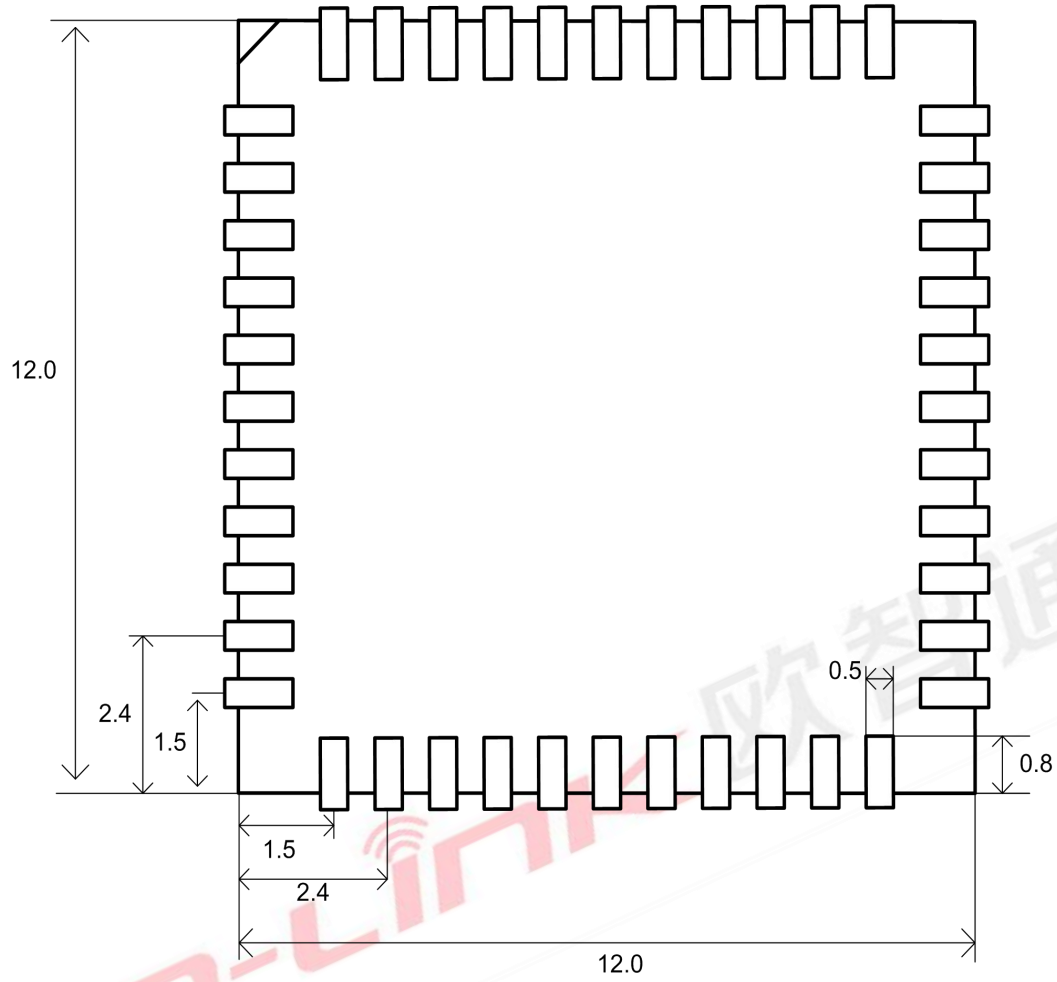
< TOP VIEW >



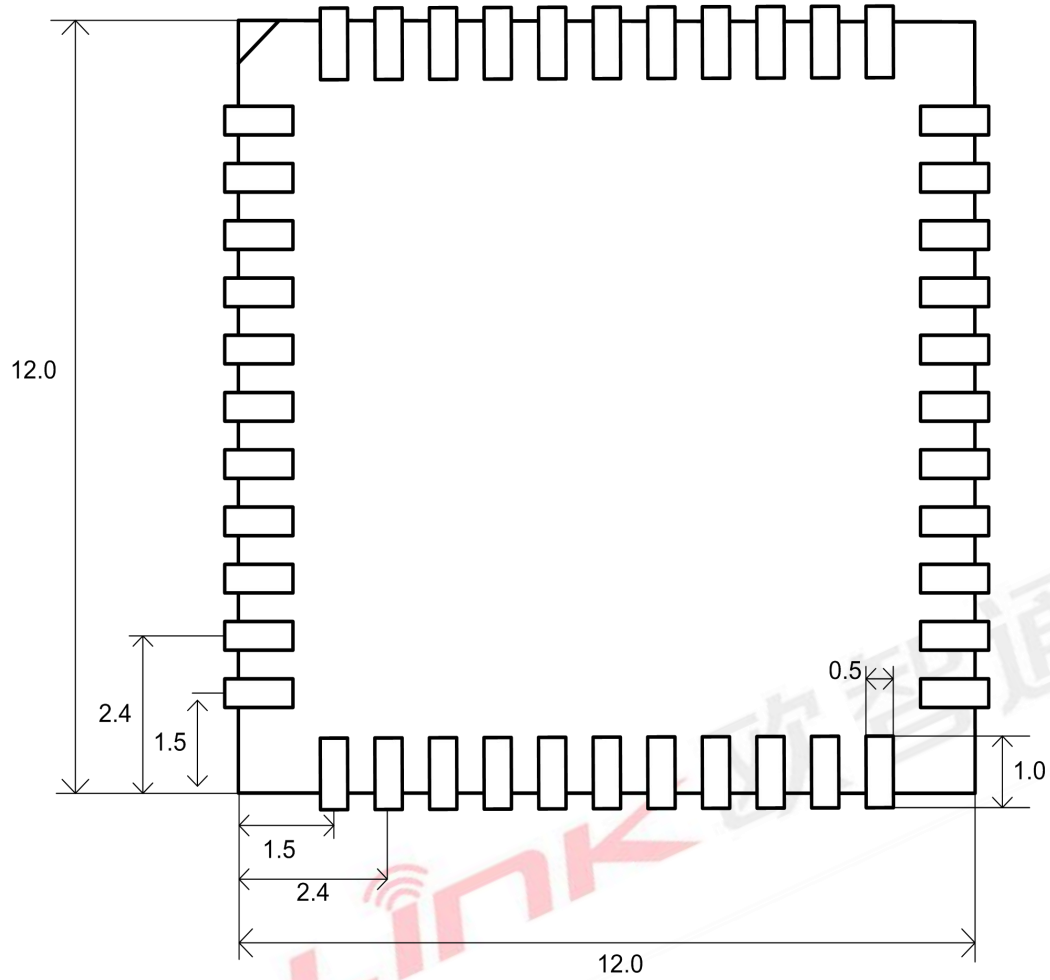
Date code: XXXX01 表示-01 机型.

7.3 Physical Dimensions

<TOP View>



7.4 Layout Recommendation

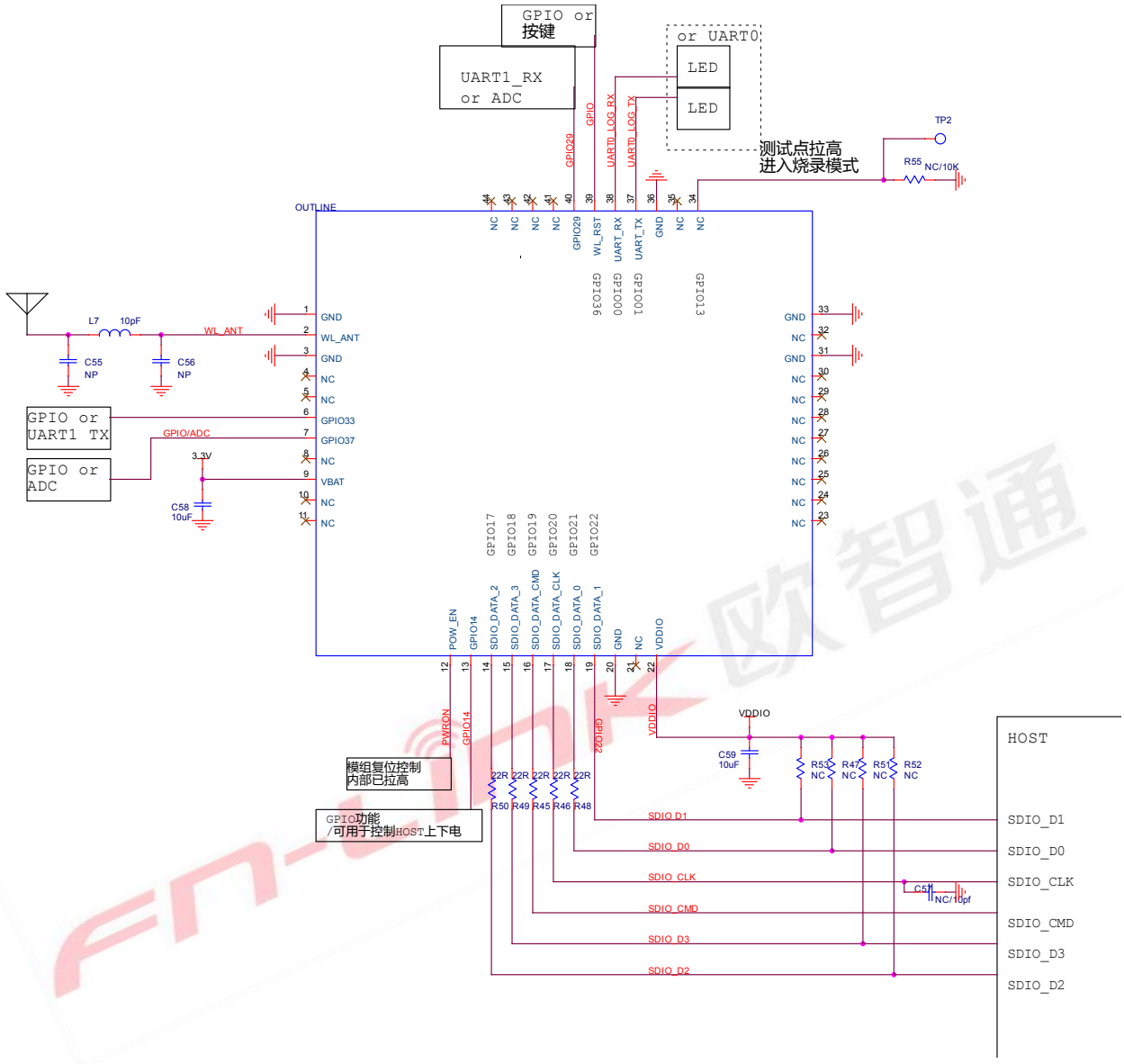


8. The Key Material List

Item	Part Name	Description	Manufacturer
1	PCB	H132A-S 4L FR4 12X12X0.8mm	XY-PCB,KX-PCB,Sunlord,SL-PCB
2	Inductor	0603,4.7uH,20%,400mA	Sunlord,cenke,ceaya
3	Shielding	H132A-S 屏蔽盖,洋白铜	信太，精力通
4	Crystal	26MHZ 3225 10PPM 9PF	TKD,ECEC,HOSONIC,JWT
5	Chipset	SV32WB01L,,QFN32	iCOMMSEMI

9. Reference Design

4line SDIO Reference Design



Note：

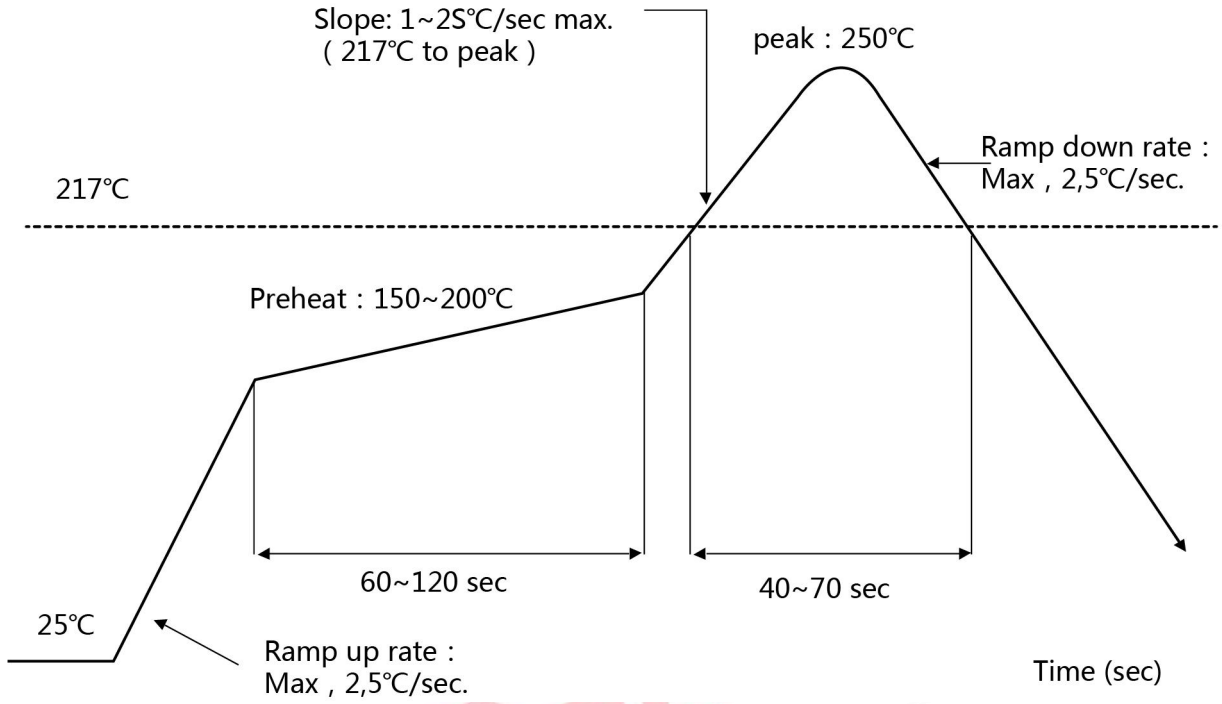
Pin34 请预留 10K 下拉；

10. Recommended Reflow Profile

Referred to IPC/JEDEC standard.

Peak Temperature : <250°C

Number of Times : ≤2 times



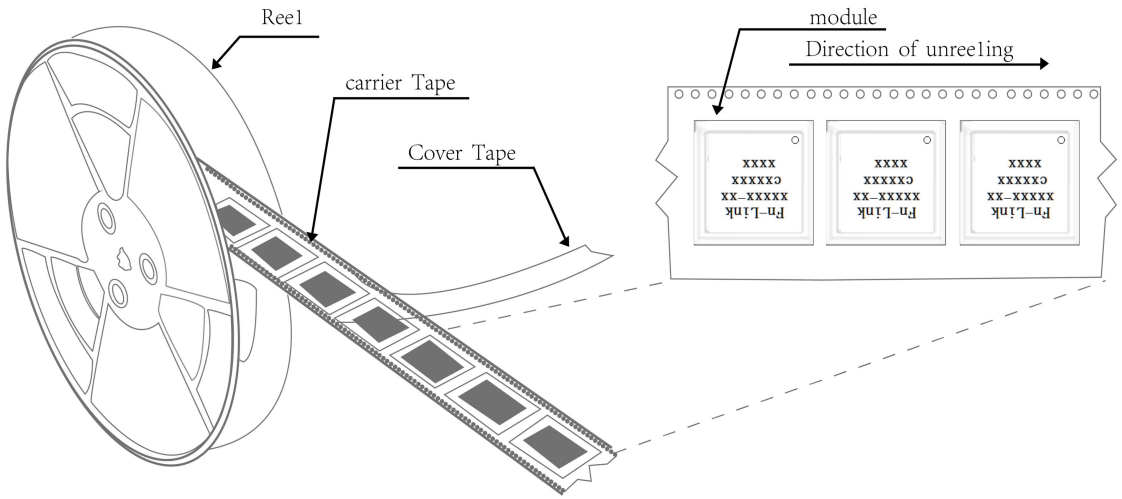
11. RoHS compliance

All hardware components are fully compliant with EU RoHS directive

12. Package

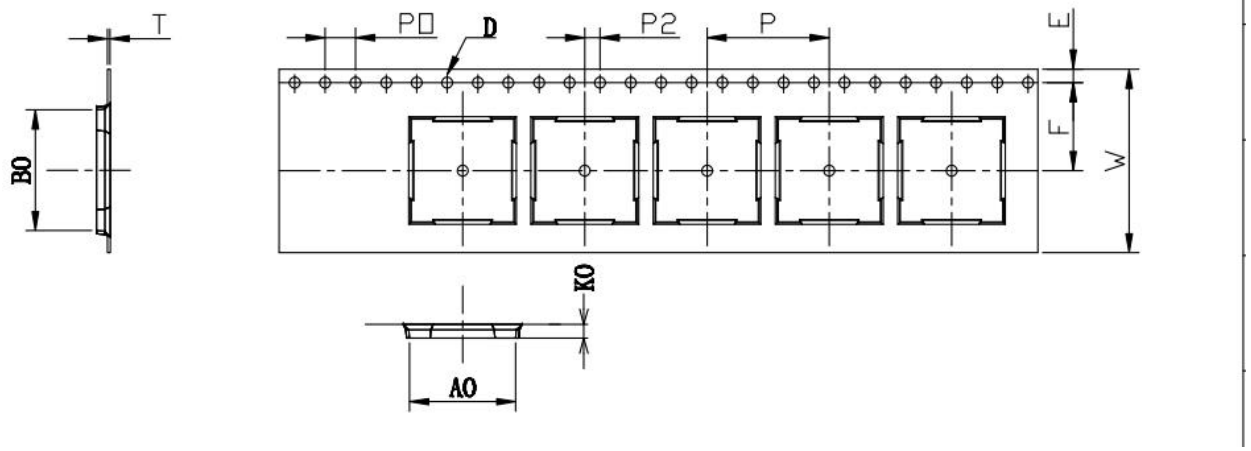
12.1 Reel

A roll of 1500pcs

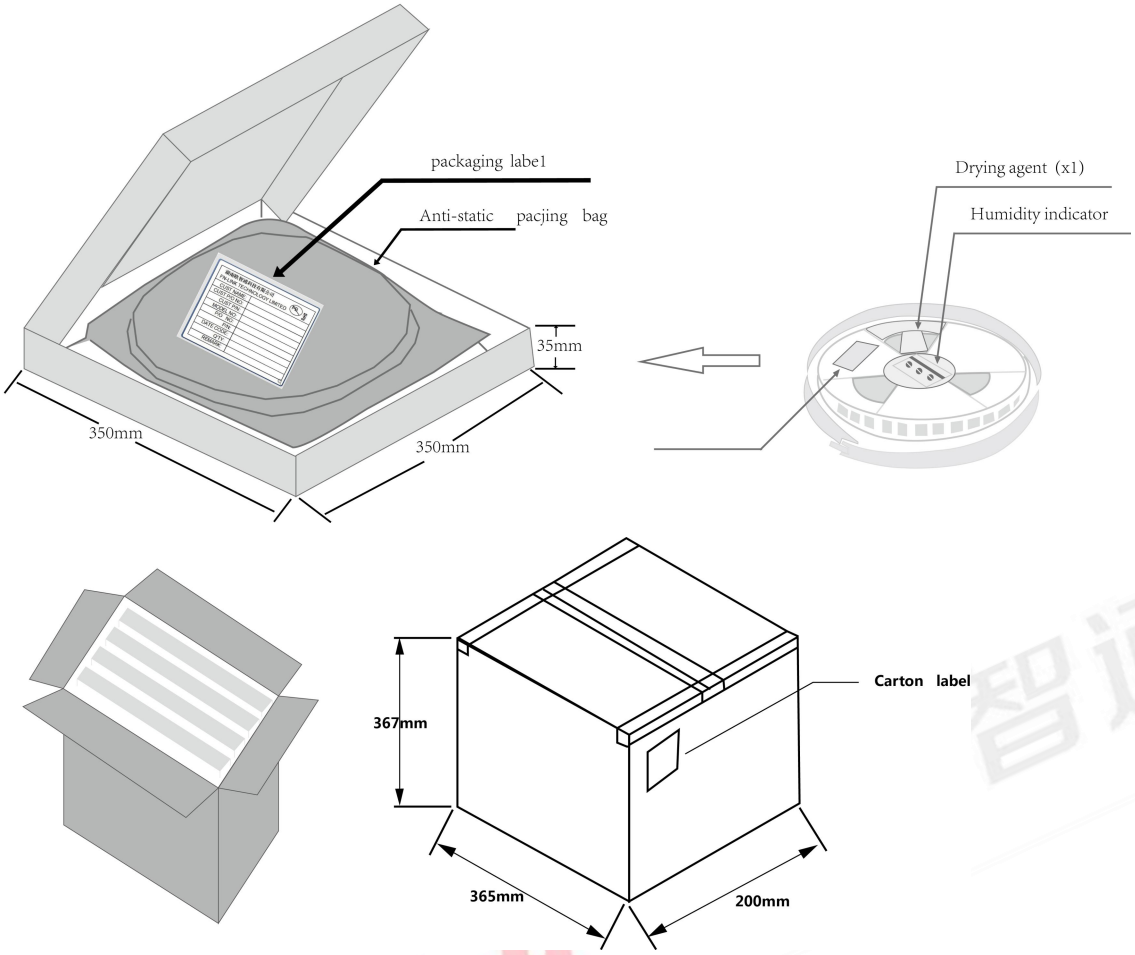


12.2 Carrier Tape Detail

ITEM	W	A0	B0	D	F	E	K0	P0	P2	P	T
DIM	24	12.45	12.45	1.50	11.5	1.75	2.60	4.0	2.0	16.0	0.30
TOLE	+0.3 -0.3	±0.15	±0.15	+0.1 -0.0	+0.1 -0.1	±0.1	±0.10	±0.1	±0.1	±0.1	±0.05



12.3 Packaging Detail



13. Moisture sensitivity

The Modules is a Moisture Sensitive Device level 3, in according with standard IPC/JEDEC J-STD-020, take care

all the relatives requirements for using this kind of components.

Moreover, the customer has to take care of the following conditions:

a) Calculated shelf life in sealed bag: 12 months at <40°C and <90% relative humidity (RH)

b) Environmental condition during the production: 30°C / 60% RH according to IPC/JEDEC J-STD-033A paragraph 5

c) The maximum time between the opening of the sealed bag and the reflow process must be 168 hours if condition

b) "IPC/JEDEC J-STD-033A paragraph 5.2" is respected

d) Baking is required if conditions b) or c) are not respected

e) Baking is required if the humidity indicator inside the bag indicates 10% RH or more