FN-LINK欧智通

# PRODUCT SPECIFICATION

# H158A-S

## Wi-Fi Single-band 1x1 802.11b/g/n + BLE5.0

## Combo Module

**Version:v1.9**

# H158A-S Module Datasheet

| | Part NO. | Description |
|---|---|---|
| **Ordering Information** | FGH158ASXX-00 | SV6158P,b/g/n,WiFi 2.4G,1T1R,SDIO,邮票孔 |
| | FGH158ASXX-01 | SV6158P,b/g/n,WiFi 2.4G,1T1R,SDIO,带天线座 |
| | FGH158ASXX-02 | SV6158P,b/g/n,WiFi 2.4G,1T1R,SDIO,邮票孔,带屏蔽盖 |
| | FGH158ASXX-03 | SV6158,b/g/n ,1T1R,12*12 ,SDIO2.0,LDO 版 |

**Customer:** _____

**Customer P/N:**_____

**Signature:**_____

**Date:**_____

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# Revision History

| Version | Date | Contents of Revision Change | Draft | Checked | Approved |
|---|---|---|---|---|---|
| V1.0 | 2020/12/23 | New version | Lxy | Lxy | SZS |
| V1.1 | 2021/3/27 | Remove shielding | Lxy | Lxy | Szs |
| V1.2 | 2021/4/6 | Upgrade tx power limit | Lxy | Lxy | Szs |
| V1.3 | 2021/6/11 | Added planeness information | Lxy | Lxy | Lgp |
| V1.4 | 2021/7/5 | Revise BLE type module P/N | Lxy | Lxy | Lgp |
| V1.5 | 2021/8/16 | Added -01 type P/N | LXY | LXY | QJP |
| V1.6 | 2021/8/30 | Added -02 type P/N | LXY | LXY | QJP |
| V1.7 | 2022/03/15 | Added -03 type P/N | Fc | LXY | QJP |
| V1.8 | 2022/05/17 | Update RX spec. | Fc | LXY | QJP |
| V1.9 | 2022/05/25 | Operating temperature updated to -40~85℃<br>update packaging information | Fc | LXY | QJP |
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# 1. General Description

## 1.1 Introduction

H158A-S is a highly integrated and excellent performance Wireless LAN (WLAN) SDIO2.0 network interface device. Based on iCOMM chipset SV6158. support 802.11b/g/n standard.

## 1.2 Description

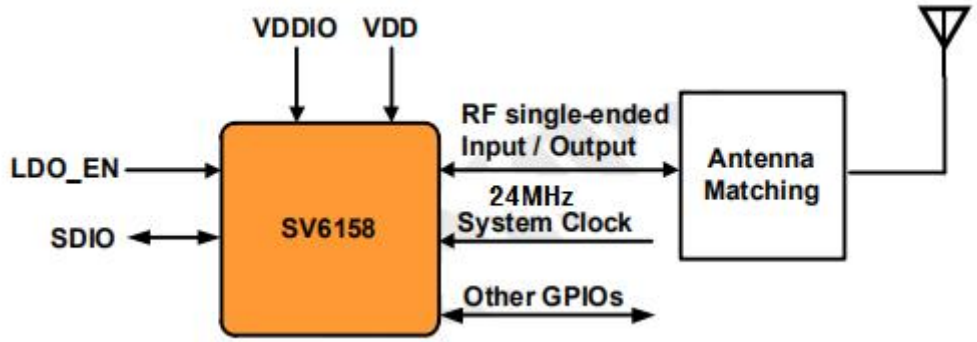
| | |
|---|---|
| Model Name | H158A-S |
| Product Description | Support Wi-Fi/Bluetooth functionalities |
| Dimension | L x W x H: 12 x 12 x1.7 mm |
| Wi-Fi Interface | Support SDIO |
| BT Interface | SDIO |
| OS supported | Android /Linux/ Win CE /iOS /XP/WIN7/WIN10 |
| Operating temperature | --40°C to 85°C |
| Storage temperature | -40°C to +85°C |

# 2. Features

### General Features

- Operate at ISM frequency bands (2.4GHz)
- CMOS MAC, Baseband PHY, and RF in a single chip for 802.11b/g/n compatible WLAN
- Wi-Fi 1 T 1 R allow data rates supporting up to 150 Mbps PHY rates
- 1bit/4bits mode supported,clock up to 50Mhz

# 3. Block Diagram




# 4. General Specification

## 4.1 WI-FI Specification

| **Feature** | **Description** | |
|---|---|---|
| WLAN Standard | IEEE 802.11 b/g/n Wi-Fi compliant | |
| Frequency Range | 2.400 GHz ~ 2.4835 GHz (2.4 GHz ISM Band) | |
| Number of Channels | 2.4GHz：Ch1 ~ Ch14 | |
| **Test Items** | **Typical Value** | **EVM** |
| Output Power | 802.11b /11Mbps : 18dBm ± 2 dB | EVM ≤ -9dB |
| | 802.11g /54Mbps : 15dBm ± 2 dB | EVM ≤ -26dB |
| | 802.11n /MCS7 : 15dBm ± 2 dB | EVM ≤ -28dB |
| | The power corresponding to other rates is configured by the driver | |
| Spectrum Mask | Meet with IEEE standard | |
| Freq. Tolerance | ±20ppm | |

| Test Items | TYP Test Value | | Standard Value |
|---|---|---|---|
| Receive Sensitivity (11b,20MHz) @8% PER | - 1Mbps | PER @ -94 dBm | ≤-83 |
| | - 2Mbps | PER @ -92 dBm | ≤-80 |
| | - 5.5Mbps | PER @ -91 dBm | ≤-79 |
| | - 11Mbps | PER @ -88 dBm | ≤-76 |
| Receive Sensitivity (11g,20MHz) @10% PER | - 6Mbps | PER @ -89 dBm | ≤-85 |
| | - 9Mbps | PER @ -88 dBm | ≤-84 |
| | - 12Mbps | PER @ -87 dBm | ≤-82 |
| | - 18Mbps | PER @ -84 dBm | ≤-80 |
| | - 24Mbps | PER @ -81 dBm | ≤-77 |
| | - 36Mbps | PER @ -78 dBm | ≤-73 |
| | - 48Mbps | PER @ -73 dBm | ≤-69 |
| | - 54Mbps | PER @ -71 dBm | ≤-68 |
| Receive Sensitivity (11n,20MHz) @10% PER | - MCS=0 | PER @ -89 dBm | ≤-85 |
| | - MCS=1 | PER @ -86 dBm | ≤-82 |
| | - MCS=2 | PER @ -84 dBm | ≤-80 |
| | - MCS=3 | PER @ -80 dBm | ≤-77 |
| | - MCS=4 | PER @ -77 dBm | ≤-73 |
| | - MCS=5 | PER @ -72 dBm | ≤-69 |
| | - MCS=6 | PER @ -71 dBm | ≤-68 |
| | - MCS=7 | PER @ -70 dBm | ≤-67 |
| Receive Sensitivity (11n,40MHz) @10% PER | - MCS=0, | PER @ -89 dBm | ≤-82 |
| | - MCS=1, | PER @ -85 dBm | ≤-79 |
| | - MCS=2, | PER @ -83 dBm | ≤-77 |
| | - MCS=3, | PER @ -80 dBm | ≤-74 |
| | - MCS=4, | PER @ -76 dBm | ≤-70 |
| | - MCS=5, | PER @ -71 dBm | ≤-66 |
| | - MCS=6, | PER @ - 70 dBm | ≤-65 |
| | - MCS=7, | PER @ -68 dBm | ≤-64 |
| Maximum Input Level | 802.11b : -10 dBm | | |
| | 802.11g/n : -20 dBm | | |
| Antenna Reference | Small antennas with 0~2 dBi peak gain | | |

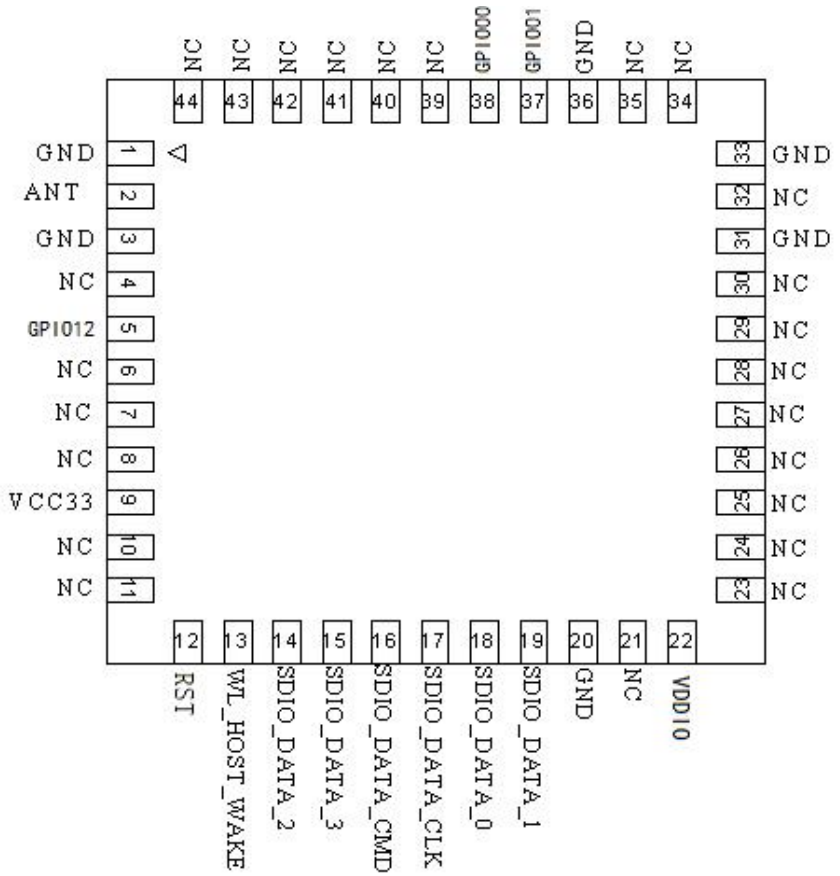
### 4.2 Bluetooth Specification

N/A

## 5. Pin Definition

### 5.1 Pin Outline

< TOP VIEW >




### 5.2 Pin Definition details

| NO. | Name | Type | Description | Voltage |
|---|---|---|---|---|
| 1 | GND | | GND | |
| 2 | ANT | I/O | RF OUTPUT | |
| 3 | GND | | GND | |
| 4 | NC | | Floating (NC) | |
| 5 | GPIO12 | I/O | Default low setting to SDIO mode,<br>pull high into SPI mode | |

| | | | | |
|---|---|---|---|---|
| 6~8 | NC | | Floating (NC) | |
| 9 | VCC33 | O | 3.3V IN | |
| 10~11 | NC | | Floating (NC) | |
| 12 | RST | | Reset, default pull high,active low | |
| 13 | WL_HOST_WAKE | | WLAN WAKE HOST,GPIO14 | |
| 14 | SDIO_DATA_2 | | SDIO_D2, GPIO17 | |
| 15 | SDIO_DATA_3 | | SDIO_D3, GPIO18 | |
| 16 | SDIO_DATA_CMD | | SDIO_CMD, GPIO19 | |
| 17 | SDIO_DATA_CLK | | SDIO_CLK, GPIO20 | |
| 18 | SDIO_DATA_D0 | | SDIO_D0, GPIO21 | |
| 19 | SDIO_DATA_D1 | | SDIO_D1, GPIO22 | |
| 20 | GND | | GND | |
| 21 | NC | | Floating (NC) | |
| 22 | VDIO | | 1.8 or 3.3V | |
| 23~30 | NC | | Floating (NC) | |
| 31 | GND | | GND | |
| 32 | NC | | Floating (NC) | |
| 33 | GND | | GND | |
| 34~35 | NC | | Floating (NC) | |
| 36 | GND | | GND | |
| 37 | GPIO01 | | UART LOG TX | |
| 38 | GPIO00 | | UART LOG RX | |
| 39~44 | NC | | Floating (NC) | |

P:POWER I:INPUT O:OUTPUT

# 6. Electrical Specifications

## 6.1 Power Supply DC Characteristics

| | MIN | TYP | MAX | Unit |
|---|---|---|---|---|
| Operating Temperature | -40 | 25 | 85 | deg.C |
| VBAT | 3.0 | 3.3 | 3.6 | V |
| VDDIO | 1.7 | 1.8 or 3.3 | 3.6 | V |

## 6.2 Power Consumption

| Vcc=3.3V, Ta=25° C, unit: mA | |
|---|---|
| 电流 | 平均值 |
| 11b 11Mbps TX mode | 186.6 |
| 11g 54Mbps TX mode | 158 |
| 11n HT20 MCS7 TX mode | 159.4 |
| 11n HT40 MCS7 TX mode | 161 |
| RX mode | 35.7 |
| Saving mode DTIM3 | 0.21 |

## 6.3 Interface Circuit time series

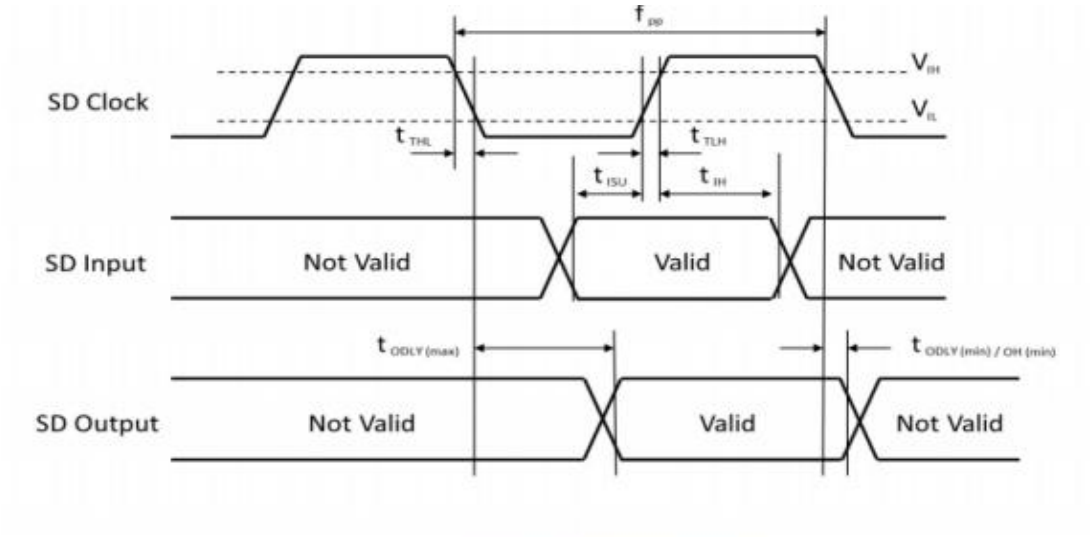
### 6.3.1 SDIO Pin Description

The module supports SDIO version 2.0 for all 1.8V 4-bit UHSI speeds: SDR12(25 Mbps), and SDR25(50Mbps) in addition to the 3.3V default speed(25MHz) and high speed (50 MHz).

SDIO Pin Description

| **SD 4-Bit Mode** | |
|---|---|
| DATA0 | Data Line 0 |
| DATA1 | Data Line 1 or Interrupt |
| DATA2 | Data Line 2 or Read Wait |
| DATA3 | Data Line 3 |
| CLK | Clock |
| CMD | Command Line |

### 6.3.2 SDIO Default Mode Timing Diagram




SDIO TIMING WAVEFORM

SDIO version 2.0 Timing Specifications

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **Clock CLK (All values are referred to min($V_{IH}$) and max ($V_{IL}$).** | | | | | |
| $f_{PP}$ | Clock frequency Data Transfer Mode | 0 | | 50 | MHz |
| $t_{TLH}$ | Clock rise time | | | 3 | ns |
| $t_{THL}$ | Clock fall time | | | 3 | ns |
| **Inputs CMD, DAT (reference to CLK)** | | | | | |
| $t_{ISU}$ | Input set-up time | 6 | | | ns |
| $t_{IH}$ | Input hold time | 2 | | | ns |
| **Outputs CMD, DAT (reference to CLK)** | | | | | |
| $t_{ODLY}$ | Output Delay time during Data Transfer Mode | | | 14 | ns |
| $t_{OH}$ | Output Hold time | 2.5 | | | Ns |

### 6.3.3 SDIO Power-on sequence

Figure 4 shows the power-on sequence of the SV615XP from power-up to firmware download, including the initial device power-on reset evoked by LDO_EN signal. The LDO_EN input level must be kept the same as VDDIO voltage level. After initial power-on, the LDO_EN signal can be held low to turn off the SV615XP or pulsed low to induce a subsequent reset. After LDO_EN is assert and host starts the power-on sequence of the SV615XP. From that point, the typical SV615XP power-on sequence is shown below:

1. Within 1.3 millisecond, the internal power-on reset (POR) will be done. And host could download firmware code of DPLL setting if the crystal is not default setting, 26MHz. The internal running clock is crystal frequency.
2. After 100us of DPLL settling time, host could set internal clock to full speed and finish all the downloading of firmware code.

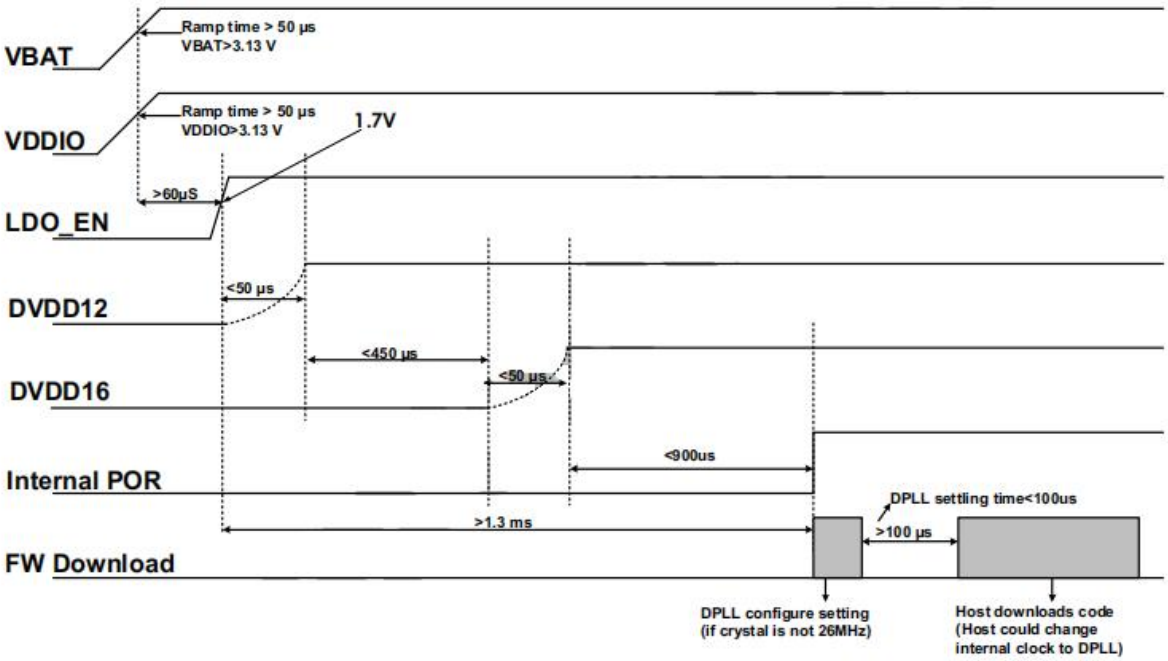



Figure 4 : Power-on sequence

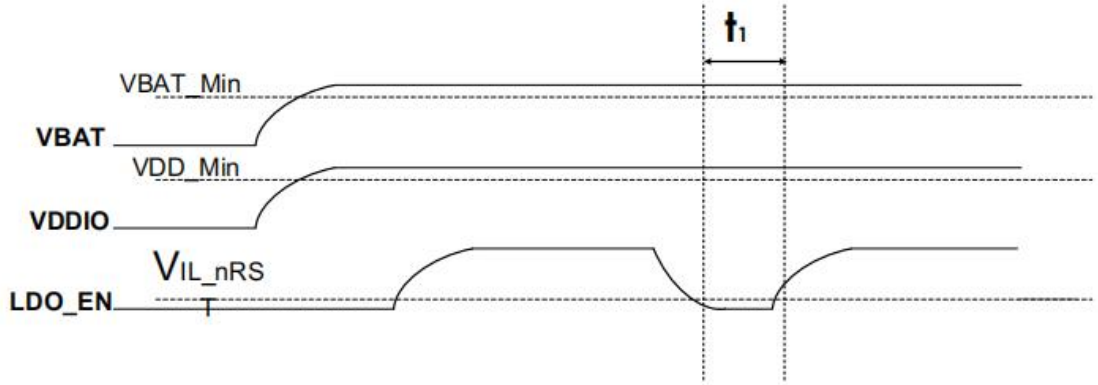



Figure 5 : Reset Timing

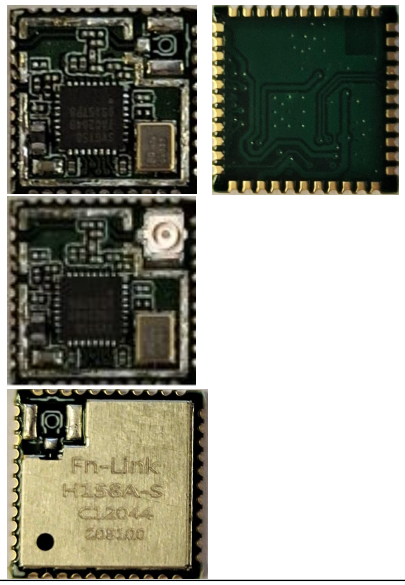
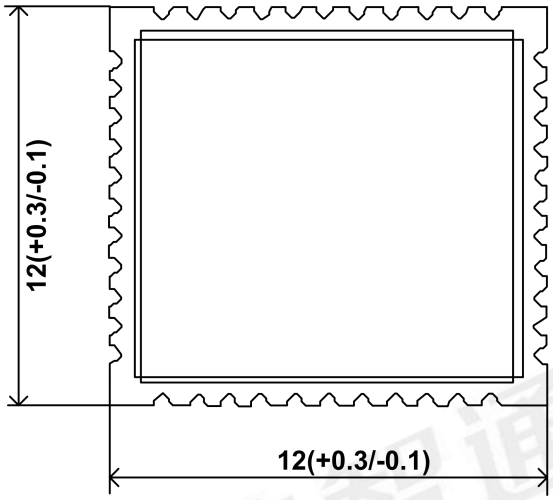
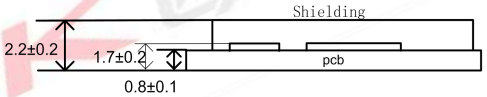
Table 2 : Reset Timing Parameters

| Parameters | Description | Min. | Unit |
|---|---|---|---|
| $t_1$ | Duration of LDO_EN signal level < $V_{IL}$_nRST to reset the chip | 30 | us |

The SV615XP LDO_EN pin can be used to completely reset the entire chip. After this signal has been de-asserted, the SV615XP is in off mode waits for host communication. Until then, the MAC, BB, and SOC blocks are powered off and all modules are held in reset. Once the host has initiated communication, the SV615XP turns on its crystal and later on DPLL. After all clocks are stable and running, the resets to all blocks are automatically de-asserted.

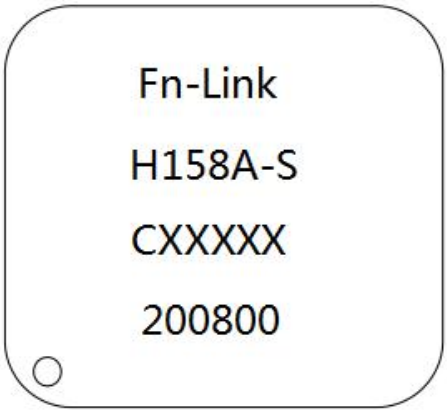
# 7. Size reference

## 7.1 Module Picture

<table>
<tr><td>L x W : 12 x 12 (+0.3/-0.1) mm<br>  </td><td>  </td></tr>
<tr><td>No shielding H: 1.7 (±0.2) mm<br>with shielding H: 2.2 (±0.2) mm</td><td>  </td></tr>
<tr><td>Weight</td><td>0.5g</td></tr>
</table>

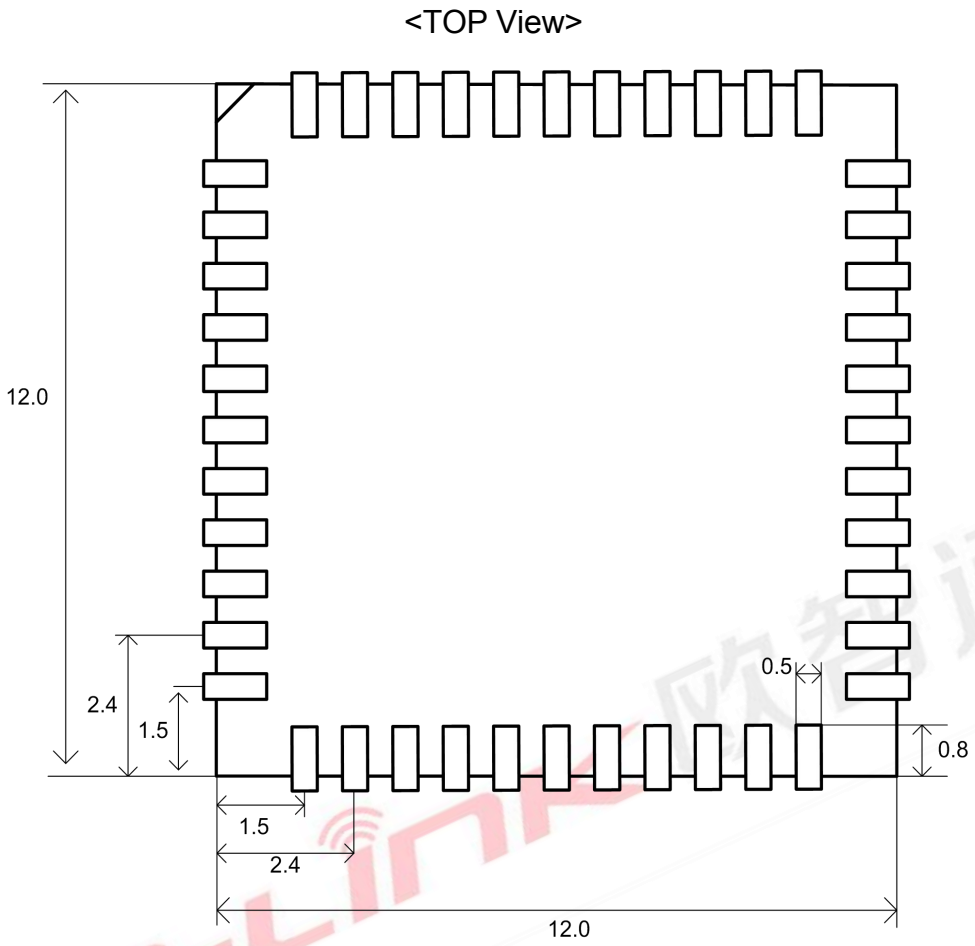
## 7.2 Marking Description

< TOP VIEW >

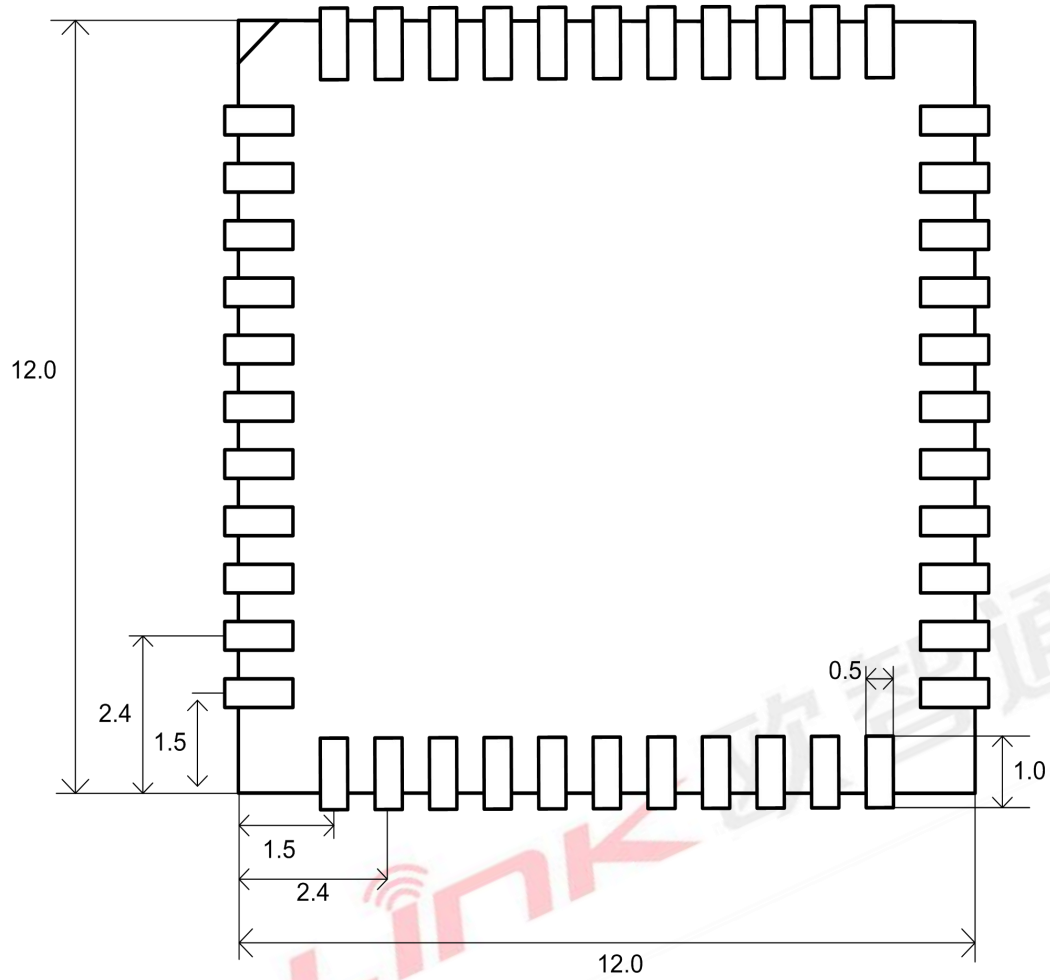



Date code last 2number means: model type

## 7.3 Physical Dimensions



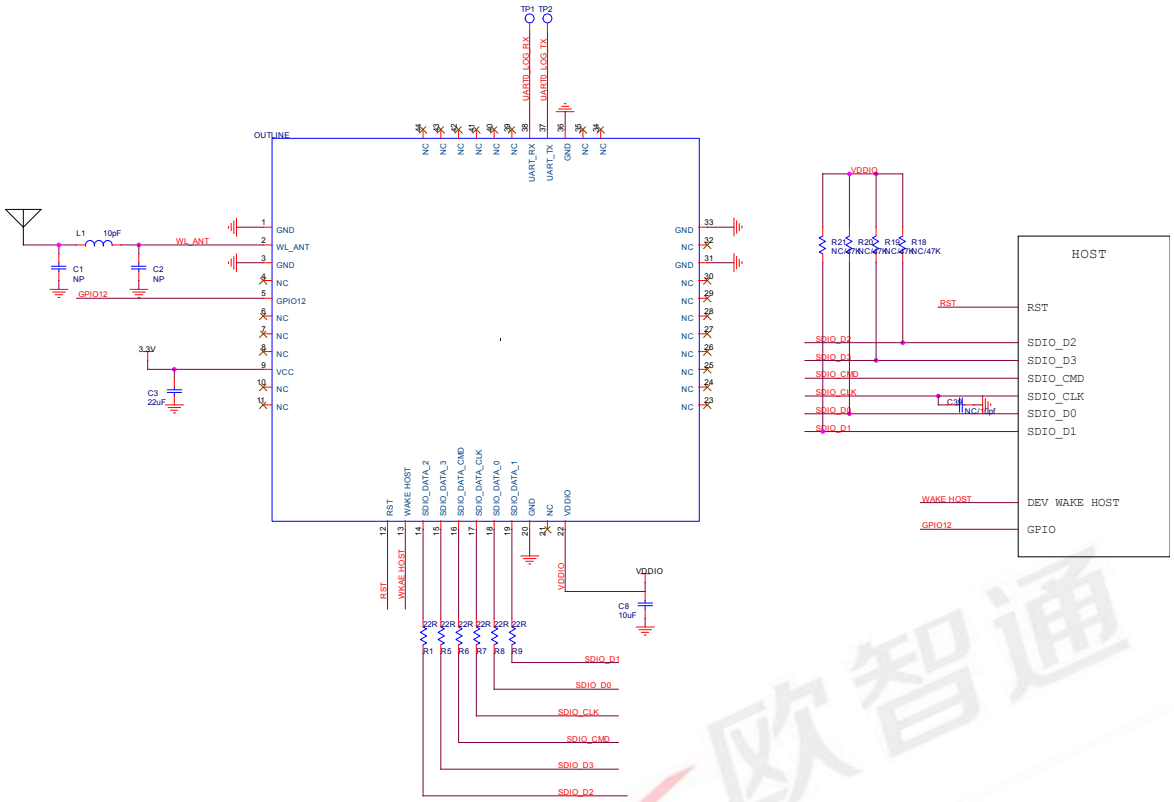
## 7.4 Layout Recommendation




# 8. The Key Material List

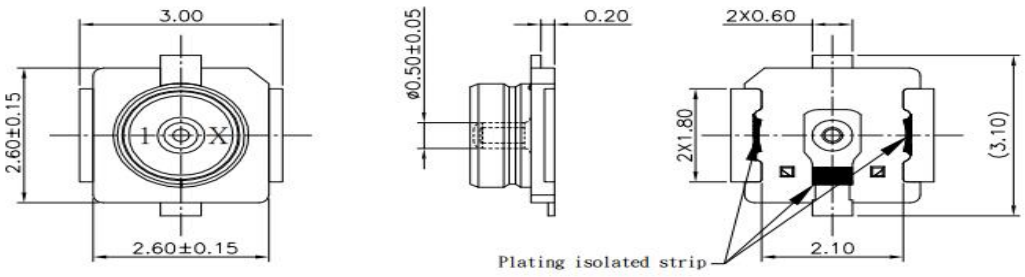
| Item | Part Name | Description | Manufacturer |
|---|---|---|---|
| 1 | Crystal | 3225 24MHZ CL=12pF,10ppm | ECEC,HOSONIC,TKD,JWT |
| 2 | PCB | H158A-S green, 4L, 12X12X0.8mm | XY-PCB,LX-PCB,SL-PCB,Sunlord |
| 3 | Chipset | SV6158, QFN32 | iCOMMSEMI |
| 4 | Inductor | 0603 4.7uH,20%,400mA | Sunlord，cenke，ceaiya |
| 5 | Shielding | H158A-S shielding | 信太，精力通 |

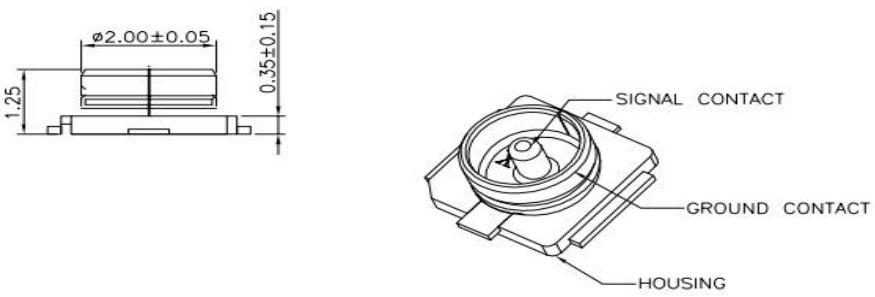
# 9. Reference Design




Note:

1. RF trace as short as possible .
2. WIth IPEX connector type，connector spec shown as below.



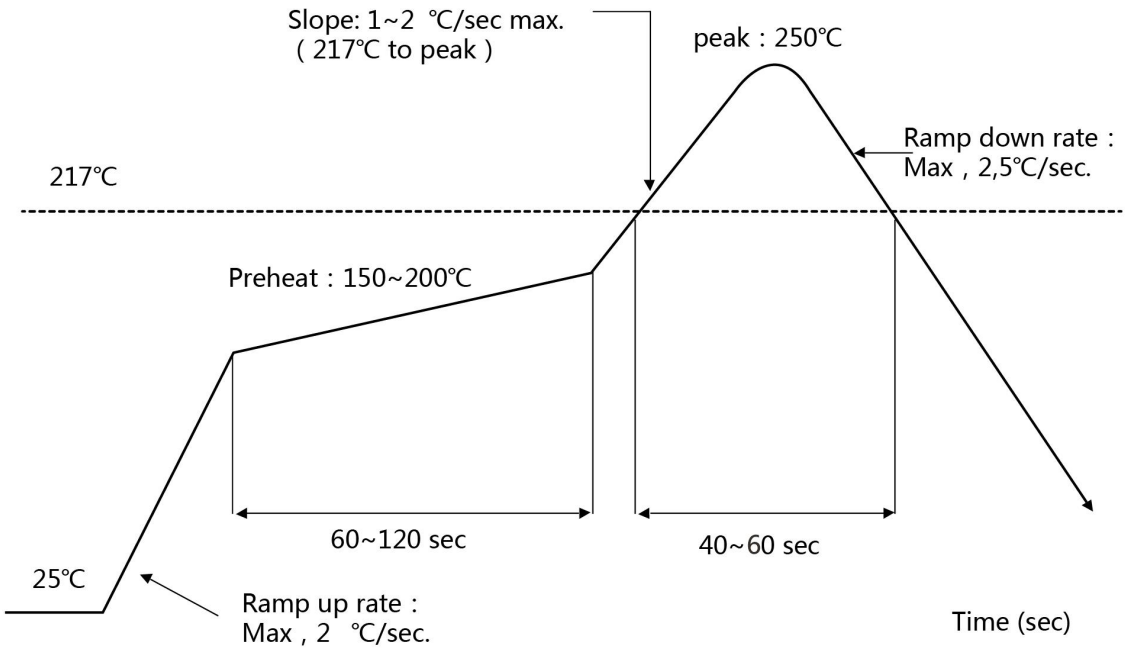



# 10. Recommended Reflow Profile

Referred to IPC/JEDEC standard.

Peak Temperature : <250°C

Number of Times : ≤2 times



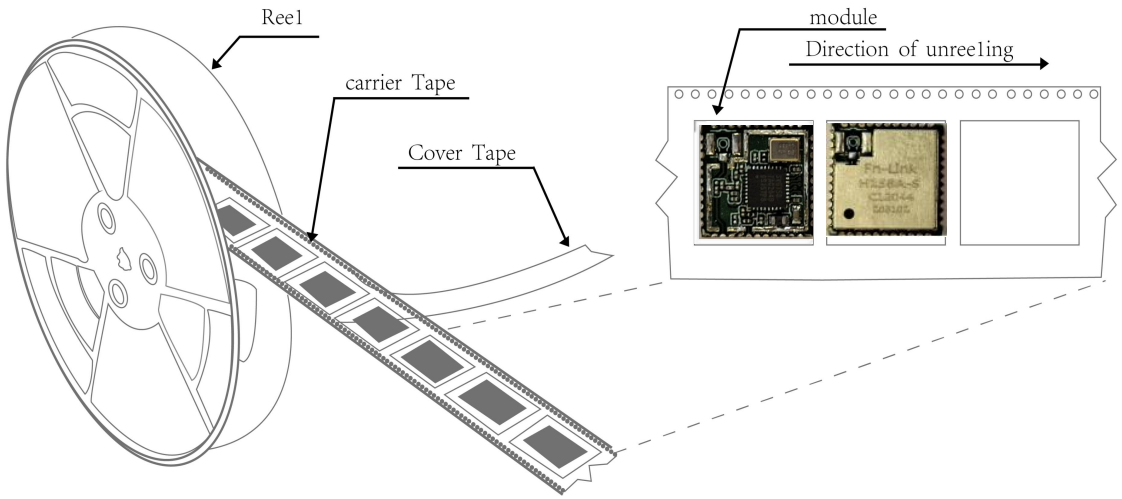

# 11. RoHS compliance

All hardware components are fully compliant with EU RoHS directive

# 12. Package

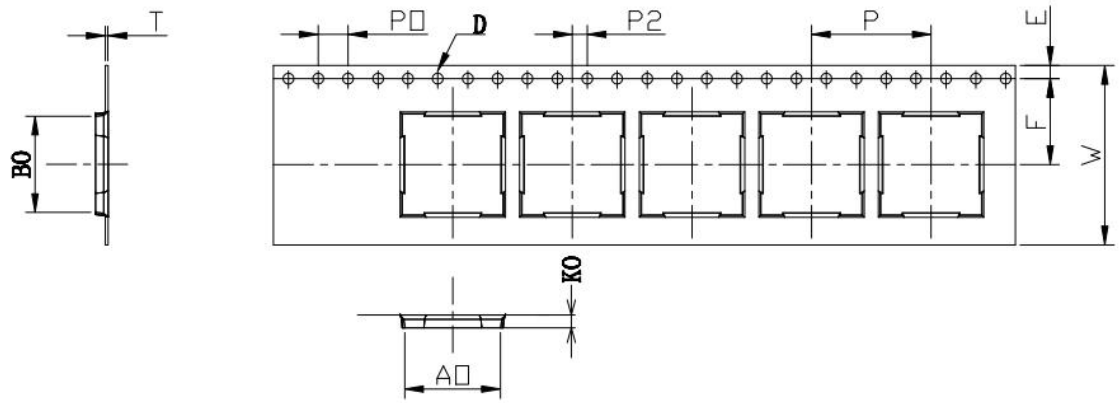
## 12.1 Reel

A roll of 1500pcs




## 12.2 Carrier Tape Detail

| ITEM | W | A0 | B0 | D | F | E | K0 | P0 | P2 | P | T |
|---|---|---|---|---|---|---|---|---|---|---|---|
| DIM | 24 | 12.45 | 12.45 | 1.50 | 11.5 | 1.75 | 2.60 | 4.0 | 2.0 | 16.0 | 0.30 |
| TOLE | +0.3 -0.3 | ±0.10 | ±0.10 | +0.1 -0.0 | +0.1 -0.1 | ±0.1 | ±0.10 | ±0.1 | ±0.1 | ±0.1 | ±0.05 |



## 12.3 Packaging Detail

the take-up package

Using self-adhesive tape

Size of black tape: 24mm*32.6m the cover tape :21.3mm*32.6m

Color of plastic disc: blue

NY bag size: 450mm*415mm size ： 350*350*35mm


The packing case size: 360*210*370mm

# 13. Moisture sensitivity

The Modules is a Moisture Sensitive Device level 3, in according with standard IPC/JEDEC J-STD-020, take care
all the relatives requirements for using this kind of components.
Moreover, the customer has to take care of the following conditions:

a) Calculated shelf life in sealed bag: 12 months at <40°C and <90% relative humidity (RH)

b) Environmental condition during the production: 30°C / 60% RH according to IPC/JEDEC J-STD-033A paragraph 5

c) The maximum time between the opening of the sealed bag and the reflow process must be 168 hours if condition

d) “IPC/JEDEC J-STD-033A paragraph 5.2” is respected

e) Baking is required if conditions b) or c) are not respected

f) Baking is required if the humidity indicator inside the bag indicates 10% RH or more