

**PRODUCT SPECIFICATION**

**H2355E-U**

**Wi-Fi Single-band 1x1 802.11b/g/n/ax +BLE 5.0**

**Module Datasheet**

Version:v1.3



## H2355E-U Module Datasheet

Ordering Information	Part NO.	Description
	FGH2355EUX-00	SV6355/2.4G/802.11b/g/n/ax+BLE5.0 1T1R,USB,12.2*13
	FGH2355EUX-01	SV6355/2.4G/802.11b/g/n/ax BLE5.0 1T1R,USB,12.2*13,带天线座版本

Customer: \_\_\_\_\_

Customer P/N: \_\_\_\_\_

Signature: \_\_\_\_\_

Date: \_\_\_\_\_

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# 1. General Description

## 1.1 Introduction

The H2355E-U is a fully integrated SoC with 2.4GHz band 1T1R 11b/g/n/ax+BLE Wi-Fi, Bluetooth Low Energy 5.0, and MCU.support Single-chip IEEE 802.11b/g/n/ax WLAN with USB Interface.

The H2355E-U WLAN SoC is designed to support IEEE 802.11 b/g/n/ax single spatial stream It is designed with the state-of-the-art techniques and process technology to achieve low power consumption and high throughput performance to address the requirement of mobile and handheld devices.

## 1.2 Description

Model Name	H2355E-U
Product Description	Support Wi-Fi functionalities
Dimension	L x W x H: 12.2 x 13 x1.62 mm
BT Interface	USB
OS supported	Android /Linux/ Win CE /iOS /XP/WIN7/WIN10
Operating temperature	0°C to 70°C
Storage temperature	-40°C to 85°C

## 2. Features

### General Features

- IEEE 802.11 b/g/n/ax+BLE5.0 compliant
- Support 802.11n 20/40MHz up to MCS7 150Mbps
- Support 802.11ax 20/40MHz up to MCS9 229Mbps
- Concurrent AP + STA supported
- including Wi-Fi WPA3, the SV6355 builds strong secure system products for smart home applications.

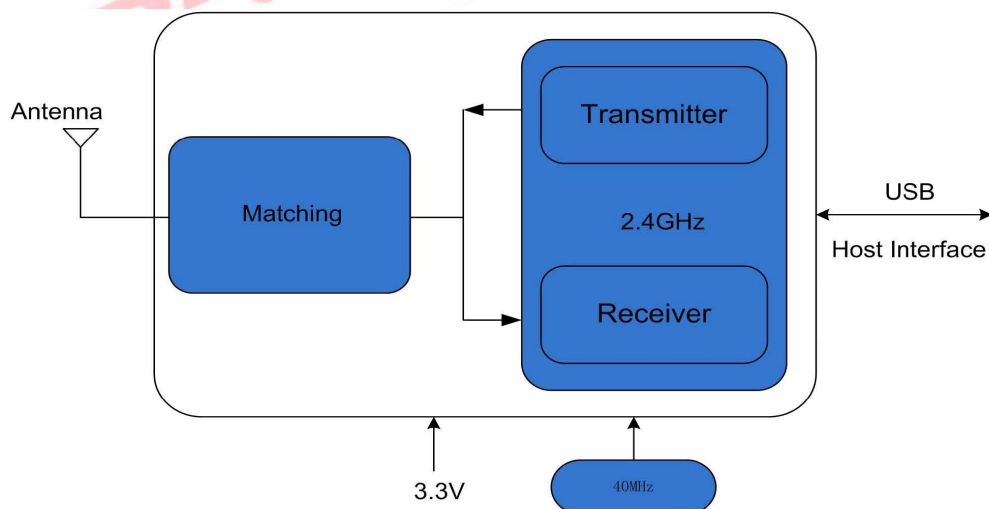
### WLAN Interface

- WiFi Support USB Interface

### Bluetooth Features

- The SV6355 supports BLE Master, Slave, Advertiser, Scanner roles. It supports standard HCI in BLE side.
- Bluetooth 5.0 Low Energy
- SIG Mesh v1.01 supported

## 3. Block Diagram



## 4. General Specification

### 4.1 WI-FI Specification

Feature	Description		
WLAN Standard	IEEE 802.11 b/g/n/ax+BLE5.0 Wi-Fi compliant		
Frequency Range	2.400 GHz ~ 2.4835 GHz (2.4 GHz ISM Band)		
Number of Channels	2.4GHz: Ch1 ~ Ch14		
Test Items	Typical Value		EVM
Output Power	802.11b /11Mbps : 17dBm ± 2 dB		EVM ≤ -9dB
	802.11g /54Mbps : 15dBm ± 2 dB		EVM ≤ -25dB
	802.11n HT40/MCS7 : 14dBm ± 2 dB		EVM ≤ -28dB
	802.11n HT20/MCS7 : 14dBm ± 2 dB		EVM ≤ -28dB
	802.11ax HE20 MCS7 : 14dBm ± 2 dB		EVM ≤ -28dB
	802.11ax HE40 MCS7 : 14dBm ± 2 dB		EVM ≤ -28dB
	802.11ax HE20 MCS9 : 12dBm ± 2 dB		EVM ≤ -32dB
	802.11ax HE40 MCS9 : 12dBm ± 2 dB		EVM ≤ -32dB
Spectrum Mask	Meet with IEEE standard		
Freq. Tolerance	± 20ppm		
Test Items	TYP Test Value		Standard Value
Receive Sensitivity (11b,20MHz) @8% PER	- 1Mbps	PER @ -92 dBm, typical	≤-85
	- 11Mbps	PER @ -85 dBm, typical	≤-76
Receive Sensitivity (11g,20MHz) @10% PER	- 6Mbps	PER @ -89 dBm, typical	≤-85
	- 54Mbps	PER @ -71 dBm, typical	≤-68
Receive Sensitivity (11n,20MHz) @10% PER	- MCS=0	PER @ -89 dBm, typical	≤-85
	- MCS=7	PER @ -69 dBm, typical	≤-67
Receive Sensitivity (11n,40MHz) @10% PER	- MCS=0	PER @ -87 dBm, typical	≤-82
	- MCS=7	PER @ -67 dBm, typical	≤-64
Receive Sensitivity (11ax,20MHz) @10% PER	- MCS=0	PER @ -82 dBm, typical	≤-78
	- MCS=9	PER @ -65 dBm, typical	≤-57
Receive Sensitivity (11ax,40MHz) @10% PER	- MCS=0	PER @ -81 dBm, typical	≤-78
	- MCS=9	PER @ -62 dBm, typical	≤-54
Maximum Input Level	802.11b : -10 dBm		
	802.11g/n : -20 dBm		
	802.11ax: -20 dBm		
Antenna Reference	Small antennas with 0~2 dBi peak gain		





## 5.2 Pin Definition details

NO.	Name	Type	Description	Voltage
1	GND	—	Ground connections	
2	ANT0	I/O	RF I/O port/version 01 NC	
3	VDD33	—	Main power voltage source input 3.3V	3.3V
4	USB_DM	I/O	USB2.0 D- for WLAN	
5	USB_DP	I/O	USB2.0 D+ for WLAN	
6	GND	—	Ground connections	

P:POWER I:INPUT O:OUTPUT

## 6. Electrical Specifications

### 6.1 Power Supply DC Characteristics

	MIN	TYP	MAX	Unit
Operating Temperature	0	25	70	deg.C
VCC33	2.1	3.3	3.46	V

### 6.2 Power Consumption

Power Consumption (Typical by using SWR)	Wi-Fi only: <b>TBD</b>
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### 6.3 Power-on sequence

Figure 3 shows the power-on sequence of from power-up to firmware download, including the initial device power-on reset evoked by internal LDO\_EN signal. After initial power-on, the LDO\_EN signal can be held low to turn off or pulsed low to induce a subsequent reset.

After LDO\_EN is asserted, the host starts the power-on sequence. From that point, the typical power-on sequence is shown below:

1. Within T1+2.5ms, the internal power-on reset (POR) will be done. And host could download firmware code of DPLL setting if the crystal is not default setting, 26MHz. The internal running clock is crystal frequency.
2. After 100us of DPLL settling time, host could set internal clock to full speed and finish all the downloading of firmware code.

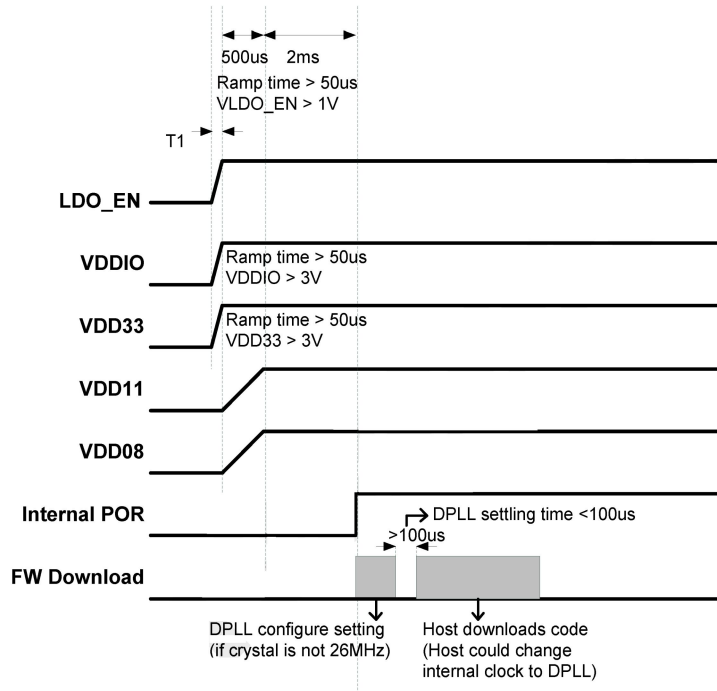


Figure 3: Power-on sequence with typical power

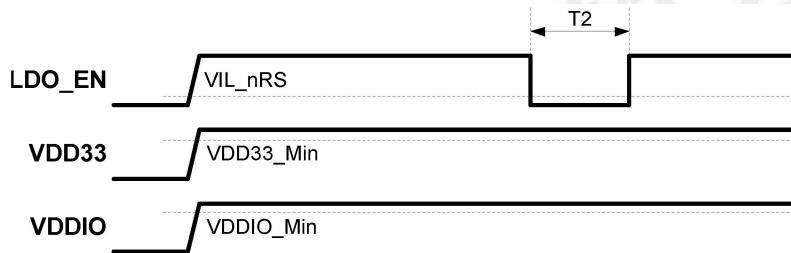


Figure 4: Reset Timing with typical power

Table 1: Reset Timing Parameters

Parameters	Description	Min.	Unit
T2	Duration of LDO_EN signal level < VIL_Nrst(refer to its value in Table 11: Recommended Operating Conditions and DC Characteristics) to reset the chip	500	us

## 6.4 Interface Circuit time series

### 6.4.1 USB CHARACTERISTICS

Table 3 : USB High-Speed Source Electrical Characteristics

Symbol	Description	Condition	Min	Typ	Max	Unit
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Driver characteristics						
tHSRLEW	Slew rate of rising edge	-	-	-	1600	V/usec
tHSRLEW	Slew rate of falling edge	-	-	-	1600	V/usec
Driver waveform	-	Specified by eye pattern template in USB2.0 spec		-	-	-
Clock Timings						
THSRDRATE	High-speed data rate	-	479.76	-	480.24	Mbps
High-Speed Data Timings						
TJ	Data source jitter	Source and receiver jitter specified by the eye pattern template defined in USB2.0 spec				
RXJT	Receiver jitter tolerance					

**Table 4: USB Full-Speed Source Electrical Characteristics**

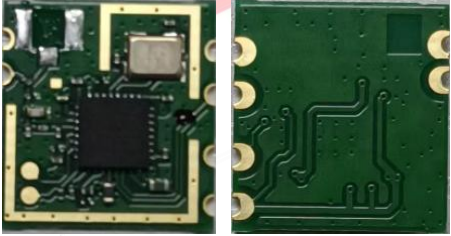
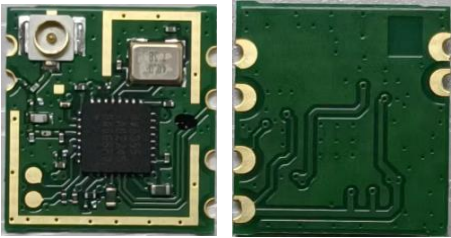
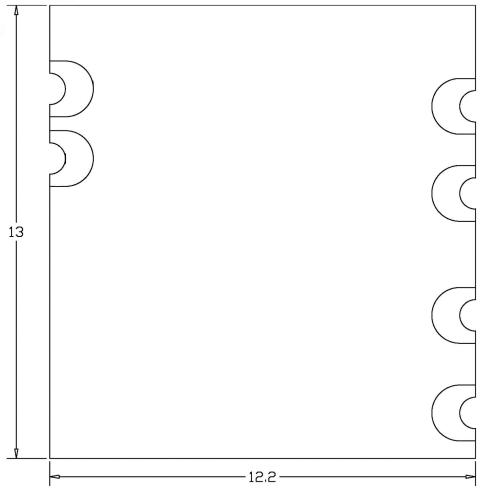
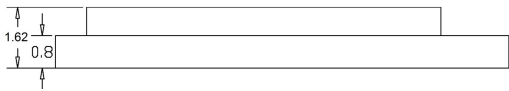
Symbol	Description	Condition	Min	Typ	Max	Unit
Driver characteristics						
tFR	Rise time	CL = 50 pF 10% ~ 90% of  VOH – VOL	4	-	20	ns
tHSFLEW	Fall time	CL = 50 pF 90% ~ 10% of  VOH – VOL	4	-	20	ns
tFRMA	Differential rise/fall time matching (tFR/tFF)	Specified by eye pattern template in USB2.0 spec	90	-	110	%
Clock Timings						
TFSTXDRATE	Full-speed TX data rate		11.994	-	12.006	Mbps
TFSRXDRATE	Full-speed RX data rate		11.97	-	12.03	Mbps
High-Speed Data Timings						
TFDEOP	Source jitter for differential transition to SEO transition	-	-2		5	ns
TJR1	Receiver jitter	To next transition	-18.5		18.5	ns
TJR2	Receiver jitter	For paired transition	-9		9	ns
TFEOPT	Source SEO interval of EOP	-	160		175	ns
TFEOPR	Receiver SEO interval of EOP	-	82		-	ns
TFST	Width of SEO interval during differential transition	-	-	-	14	ns

**Table 5 : USB Low-Speed Source Electrical Characteristics**

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
<b>Driver characteristics</b>						
tFR	Rise time	CL = 200 pF ~ 600 pF 10% ~ 90% of  VOH-VOL	75	-	300	ns
tHSFLEW	Fall time	CL = 200pF ~ 600pF 90% ~ 10% of  VOH-VOL	75	-	300	ns
tFRMA	Differential rise/fall time matching (tFR/tFF)	Specified by eye pattern template in USB2.0 spec.	80	-	125	%
<b>Clock Timings</b>						
TFSTXDRATE	Low-speed TX data rate		1.49925	-	1.50075	Mbps
TFSRXDRATE	Low-speed RX data rate		1.49925	-	1.50075	Mbps
<b>Low-Speed Data Timings</b>						
TFDEOP	Source jitter for differential transition to SE0 transition	-	-40	-	100	ns
TJR1	Receiver jitter	To next transition	-75	-	75	ns
TJR2	Receiver jitter	For paired transition	-45	-	45	ns
TFEOPT	Source SE0 interval of EOP	-	1.25	-	1.5	ns
TFEOPR	Receiver SE0 interval of EOP	-	670	-	-	ns
TFST	Width of SE0 interval during differential transition	-	-	-	210	ns

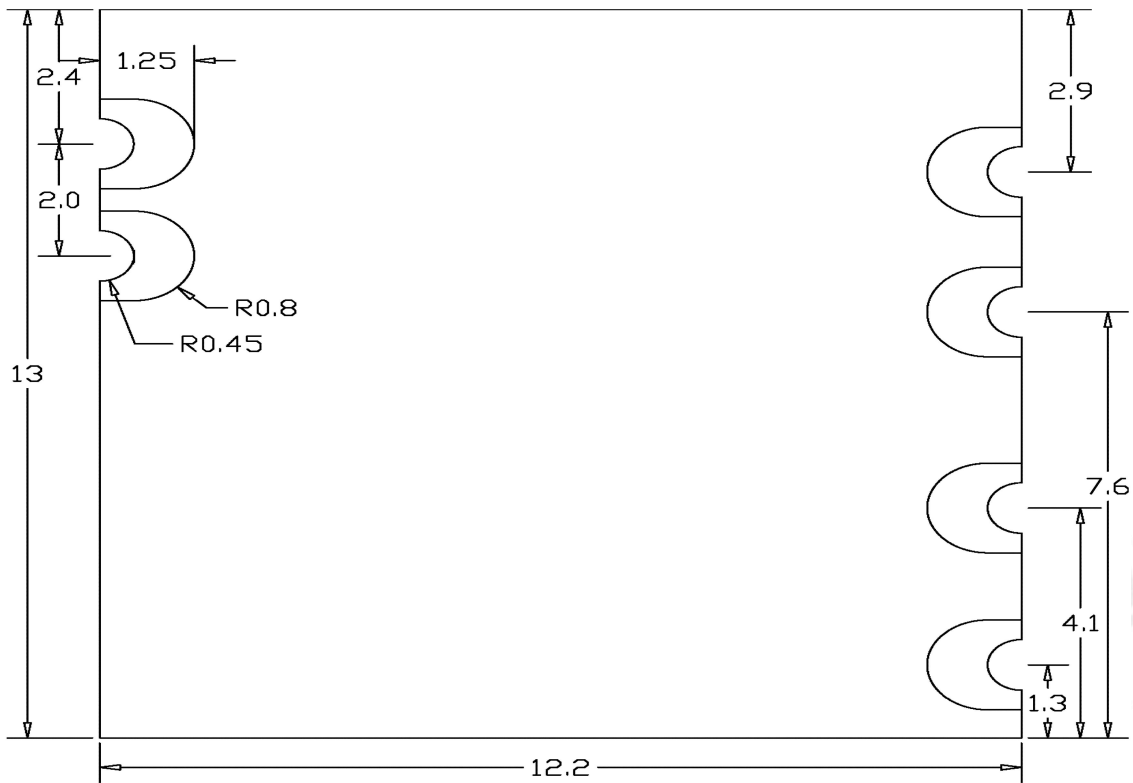
## 7. Size reference

### 7.1 Module Picture

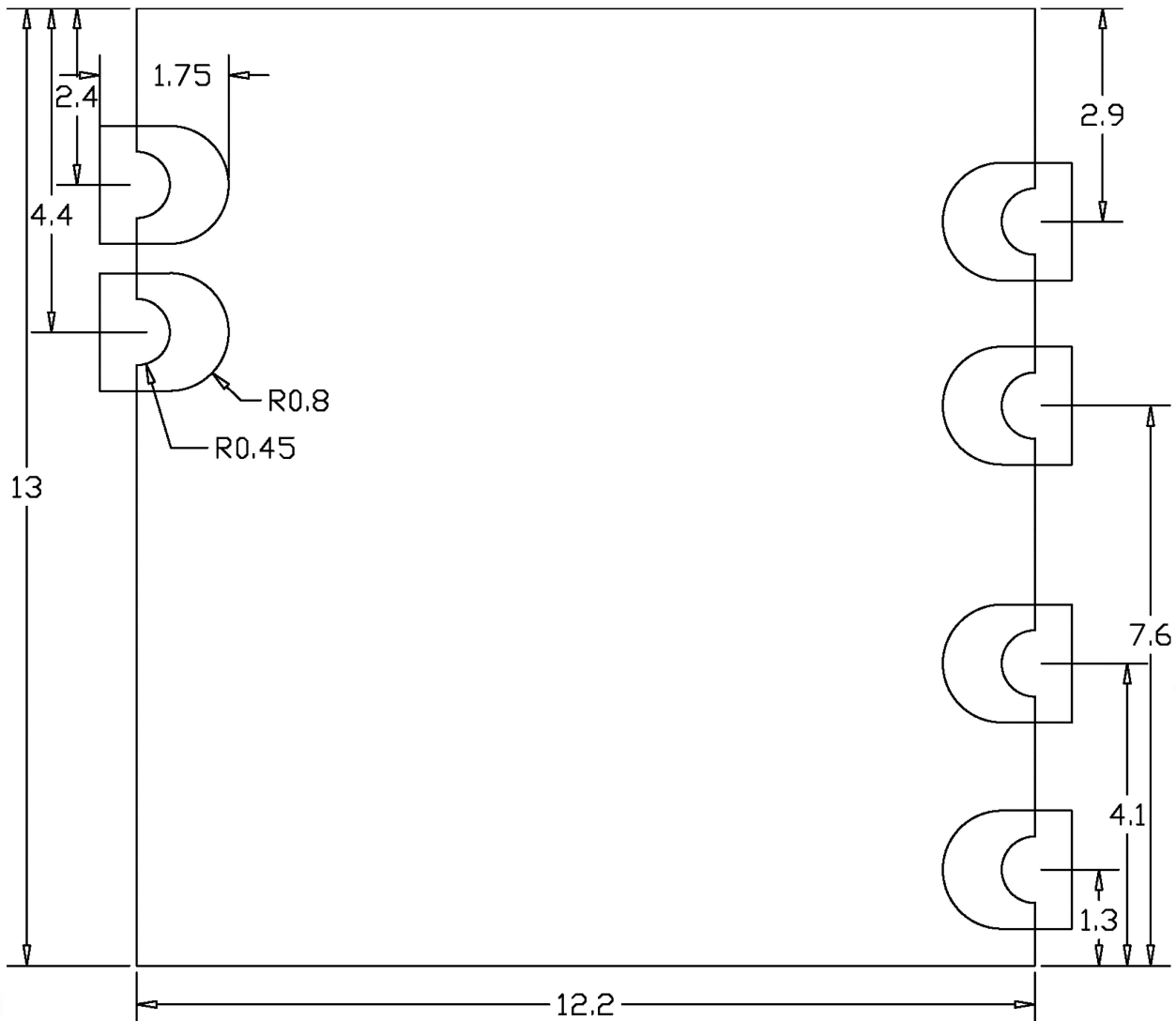
<p><b>L x W : 12.2 x 13 (+0.3/-0.1) mm</b></p> <p>FGH2355EUX-00</p>  <p>FGH2355EUX-01</p> 	
<p><b>H: 1.62 (±0.2) mm</b></p>	
<p><b>Weight</b></p>	<p><b>0.42g</b></p>

**7.2 Physical Dimensions**

<TOP View>



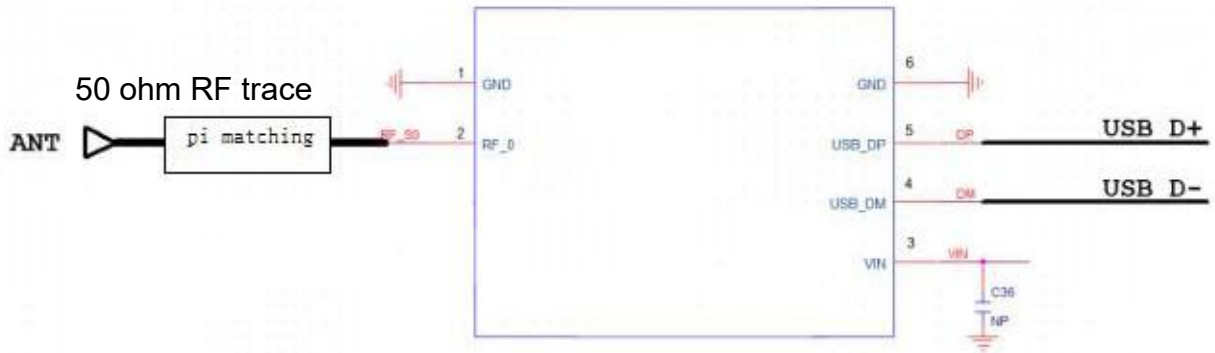
### 7.3 Layout Recommendation



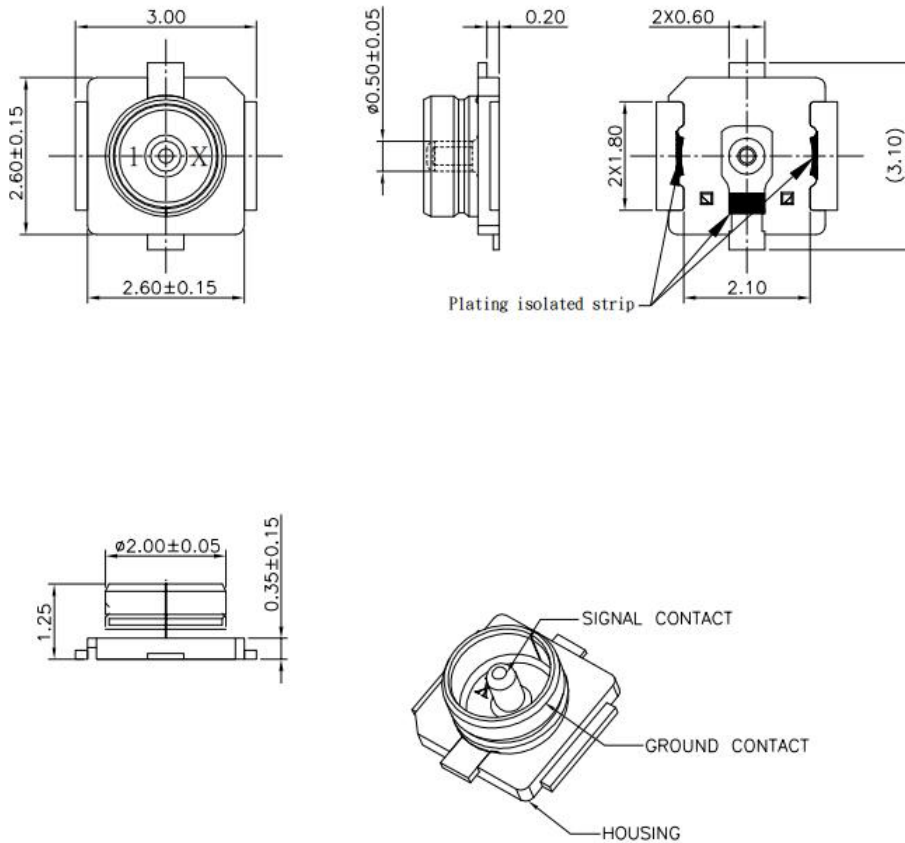
### 8. The Key Material List

Item	Part Name	Description	Manufacturer
1	PCB	H2355E-U 绿色,4L,FR4,,13x12.2x0.8mm	XY-PCB, GDKX, Sunlord, SLPCB, TRULY
2	Crystal	3225 40MHz,9pF,±10ppm	ECEC, Hosonic, TKD, JWT
3	Chipset	SV6355,iComm,QFN32L	南方硅谷

## 9. Reference Design



天线座版规格

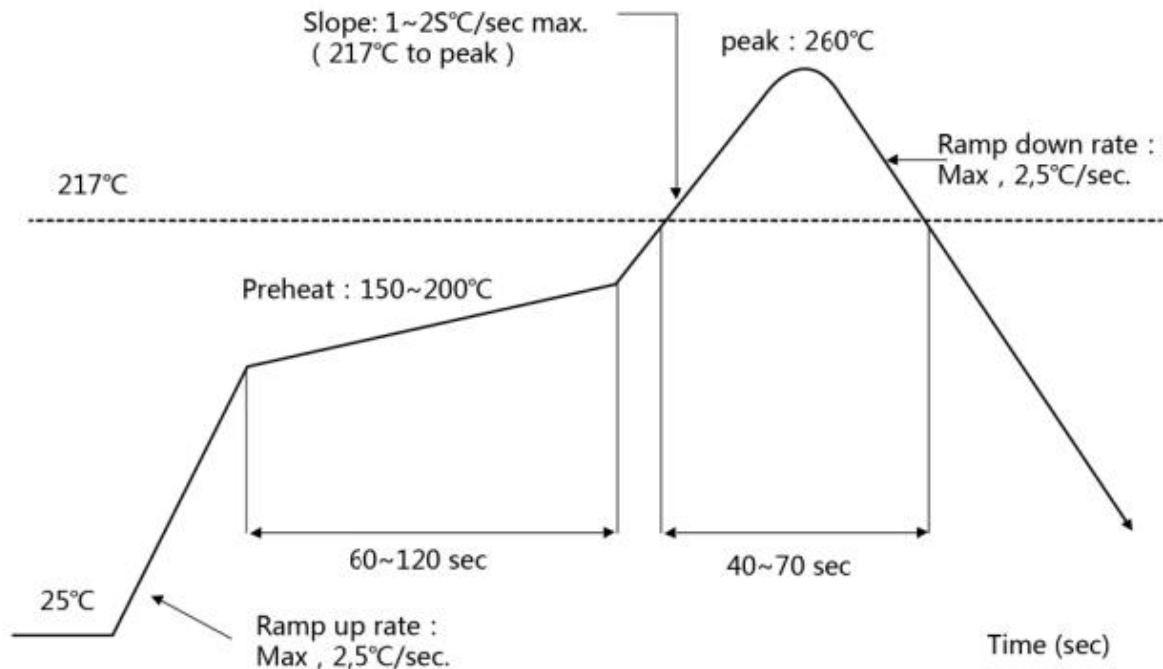


## 10. Recommended Reflow Profile

Referred to IPC/JEDEC standard.

Peak Temperature : <260°C

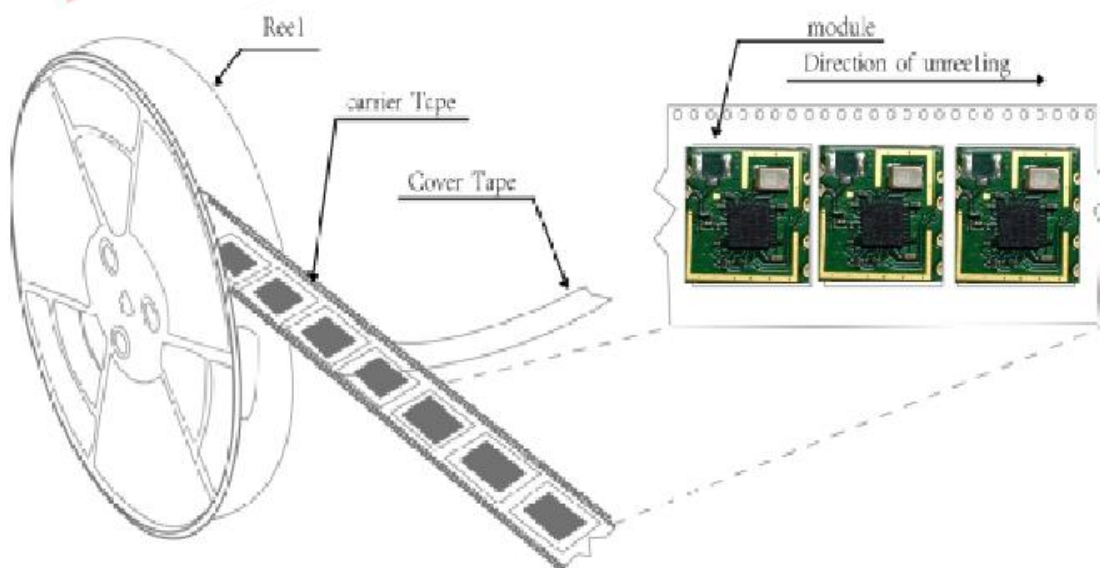
Number of Times : ≤2 times



## 11. Package

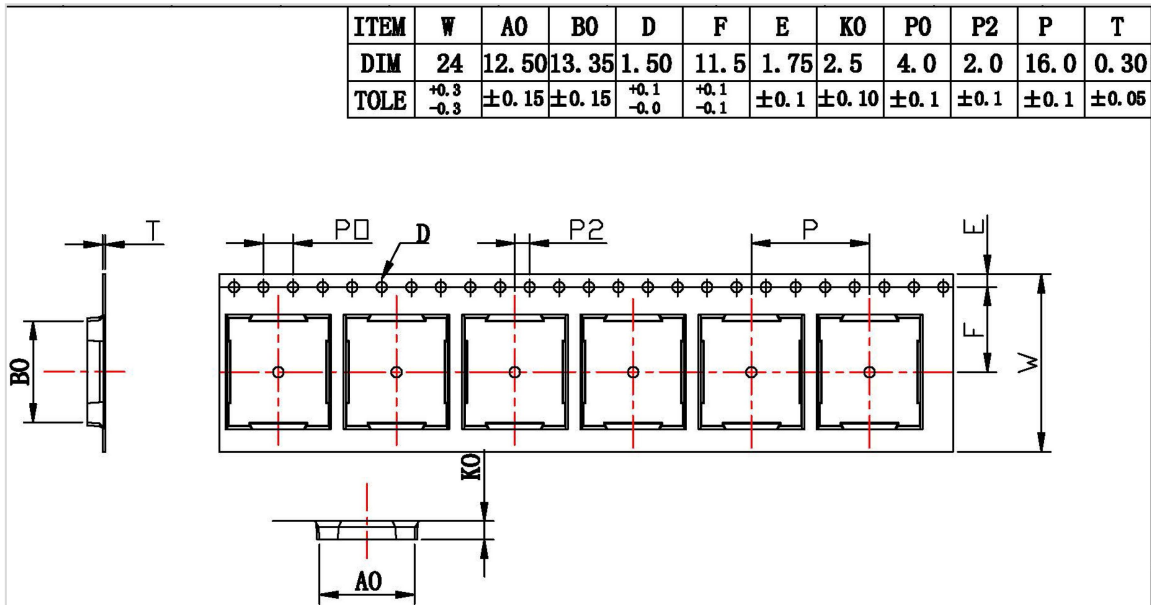
### 11.1 Reel

A roll of 1500pcs





### 11.2 Carrier Tape Detail



### 11.3 Packaging Detail

the take-up package



Using self-adhesive tape

Size of black tape: 24mm\*24.4m the cover tape :21.3mm\*32.6m

Color of plastic disc: blue



NY bag size:450mm\*415mm



size : 350\*350\*35mm



The packing case size:360\*210\*370mmg

## 12. Moisture sensitivity

The Modules is a Moisture Sensitive Device level 3, in according with standard IPC/JEDEC J-STD-020, take care

all the relatives requirements for using this kind of components.

Moreover, the customer has to take care of the following conditions:

- a) Calculated shelf life in sealed bag: 12 months at <40°C and <90% relative humidity (RH)
- b) Environmental condition during the production: 30°C / 60% RH according to IPC/JEDEC J-STD-033A paragraph 5
- c) The maximum time between the opening of the sealed bag and the reflow process must be 168 hours if condition
- d) "IPC/JEDEC J-STD-033A paragraph 5.2" is respected
- e) Baking is required if conditions b) or c) are not respected
- f) Baking is required if the humidity indicator inside the bag indicates 10% RH or more