FN-LINK 欧智通

PRODUCT SPECIFICATION

J102L-R

Wi-Fi Single-band 1x1 802.11b/g/n + BLE 5.0

Combo Module

Version:v1.0

J102L-R Module Datasheet

	Part NO.	Description
Ordering Information	FGJ102LRX-00	BL602C-20-Q2I /802.11b/g/n/ WiFi + BLE 5.0, 1T1R , UART, antenna on board, 25mm*31mm,finished product.

Customer: _____

Customer P/N:_____

Signature:_____

Date:_____

Office: 14th floor, Block B, phoenix zhigu, Xixiang Street, Baoan District, Shenzhen

Factory: NO.8, Litong RD., Liuyang Economic & Technical Development Zone, Changsha, CHINA

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CONTENTS

Revision History

Version	Date	Contents of Revision Change	Preparde	Checked	Approved
V1.0	2021/11/25	New version	FC	ZZQ	QJP

1. General Description

1.1 Introduction

Fn-Link J102L-R is a wireless module based on WiFi + BLE single chip SOC BL602C, which can meet the requirements of low power consumption and high performance IOT. The core processor BL602C integrates the baseband and MAC design of 2.4G WiFi (802.11b/g/n) and BLE 5.0.The micro-controller subsystem consists of a low-power 32-bit RISC CPU, cache and memory.

With advanced power management unit, Fn-Link J102L-R support a variety of low power consumption modes. The program can be downloaded and burned directly through UART.

1.2 Description

Model Name	J102L-R
Product Description	Support Wi-Fi/BLE
Dimension	L x W x H: 25x 31 x 3.5 (typical) mm
Wi-Fi Interface	Support SDIO/UART
BT Interface	UART
Operating temperature	-20℃ to +85℃
Storage temperature	-55℃ to +85℃

2. Features

General

- 802.11b/g/n compatible WLAN
- Wi-Fi Security WPS / WEP / WPA / WPA2 Personal / WPA2 Enterprise / WPA3
- Wi-Fi fast connection with BLE assistance

PHY Features

- 72.2Mbps transmit and receive PHY rate using 20MHz bandwidth
- Support STA and SoftAP, STA+SoftAP and sniffer modes

MCU Features

- 32-bit RISC CPU with FPU
- RAM 276KB
- ROM 128KB
- Flash 2MB
- Build-In 32KHz RTC

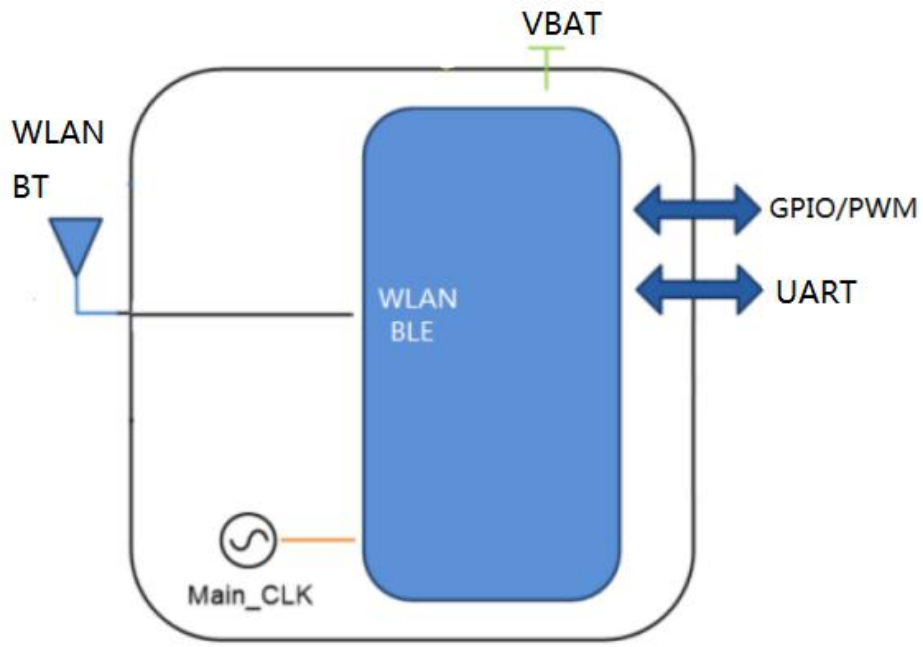
Host Interface

- Support UART Interface
- Support PWM Interface

Bluetooth Features

- Wi-Fi and BLE coexistence
- Bluetooth® Low Energy 5.0
- BLE 5.0 Channel Selection#2 is supported

3. Block Diagram



4. General Specification

4.1 WI-FI Specification

Feature	**Description**	
WLAN Standard	IEEE 802.11 b/g/n Wi-Fi compliant	
Frequency Range	2.400 GHz ~ 2.4835 GHz (2.4 GHz ISM Band)	
Number of Channels	2.4GHz：Ch1 ~ Ch14	
Test Items	**Typical Value**	**EVM**
Output Power	802.11b /11Mbps : 18dBm ± 2 dB	EVM ≤ -9dB
	802.11g /54Mbps : 14dBm ± 2 dB	EVM ≤ -25dB
	802.11n /MCS7 : 14dBm ± 2 dB	EVM ≤ -28dB
Spectrum Mask	Meet with IEEE standard	
Freq. Tolerance	±20ppm	
SISO Receive Sensitivity (11b,20MHz) @8% PER	- 1Mbps PER @ -92 dBm	≤-83
	- 11Mbps PER @ -85 dBm	≤-76

SISO Receive Sensitivity (11g,20MHz) @10% PER	- 6Mbps	PER @ -89 dBm	≤-85
	- 54Mbps	PER @ -70 dBm	≤-68
SISO Receive Sensitivity (11n,20MHz) @10% PER	- MCS=0	PER @ -89 dBm	≤-85
	- MCS=7	PER @ -68 dBm	≤-67

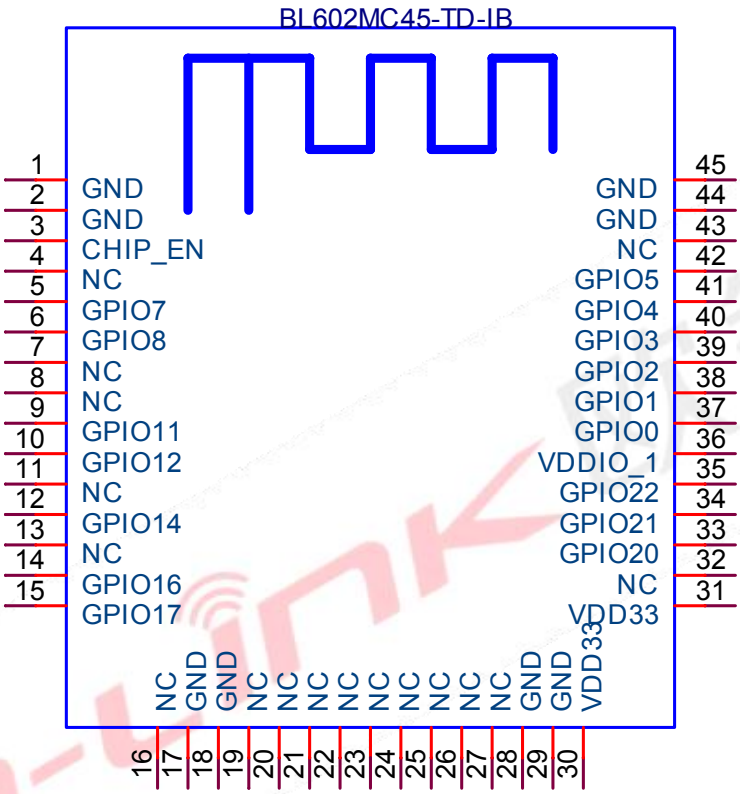
4.2 Bluetooth Specification

Feature	**Description**		
General Specification			
Bluetooth Standard	BLE 5.0 of 1Mbps.		
Host Interface	UART		
Antenna Reference	Small antennas with 0~2 dBi peak gain		
Frequency Band	2402 MHz ~ 2480 MHz		
Number of Channels	39 channels		
RF Specification			
	Min(dBm)	**Typical**(dBm)	**Max**(dBm)
Output Power (Class 1)	0	6	15
Sensitivity @ BER=0.1% for GFSK (1Mbps)			-70
Maximum Input Level	GFSK (1Mbps):-20dBm		

5. Pin Definition

5.1 Pin Outline

< TOP VIEW



5.2 Pin Definition details

NO.	Name	Type	Description	Voltage
1	GND	P	Ground connections	
2	GND	P	Ground connections	
3	CHIP_EN	I	Power enable of module ON: pull high ; OFF: pull low	
4	NC		Floating (NC)	
5	GPIO7	I	RXD，default module Programming pins	

	6	GPIO8	I/O	Boot pin, module startup mode control pin,default pull-down	
	7	NC		Floating (NC)	
	8	NC		Floating (NC)	
	9	GPIO11	I/O	GPIO Pin. The MUX Function can be referred to Pin Function Table	
	10	GPIO12	I/O	GPIO Pin. The MUX Function can be referred to Pin Function Table	
	11	NC		Floating (NC)	
	12	GPIO14	I/O	GPIO Pin. The MUX Function can be referred to Pin Function Table	
	13	NC		Floating (NC)	
	14	GPIO16	O	TXD，default module Programming pins	
	15	GPIO17	I/O	GPIO Pin. The MUX Function can be referred to Pin Function Table	
	16	NC		Floating (NC)	
	17	GND	P	Ground connections	
	18	GND	P	Ground connections	
	19~27	NC		Floating (NC)	
	28~29	GND	P	Ground connections	
	30-31	VDD33	P	3.3V Input	
	32	NC		Floating (NC)	
	33	GPIO20	I/O	GPIO Pin. The MUX Function can be referred to Pin Function Table	
	34	GPIO21	I/O	GPIO Pin. The MUX Function can be referred to Pin Function Table	
	35	GPIO22	I/O	GPIO Pin. The MUX Function can be referred to Pin Function Table	
	36	VDDIO_1	P	3.3V /1.8VInput	
	37	GPIO0	I/O	GPIO Pin. The MUX Function can be referred to Pin Function Table	
	38	GPIO2	I/O	GPIO Pin. The MUX Function can be referred to Pin Function Table	
	39	GPIO2	I/O	GPIO Pin. The MUX Function can be referred to Pin Function Table	
	40	GPIO3	I/O	GPIO Pin. The MUX Function can be referred to Pin Function Table	
	41	GPIO4	I/O	GPIO Pin. The MUX Function can be referred to Pin	

			Function Table	
42	GPIO5	I/O	GPIO Pin. The MUX Function can be referred to Pin Function Table	
43	NC		Floating (NC)	
44~45	GND	P	Ground connections	

P:POWER I:INPUT O:OUTPUT

GPIO8 is module startup mode control pin, pull down when reset, the module starts normally（tacitly approve）;pull up when reset，module enters burn mode.

5.3 Pin Function Group Table

Pin #	Name	Flash	SDIO	SPI	UART(Default/SWAP=1)	I2C Master	PWM	Analog	External_PA	JTAG (Default/SWAP=1)
13	GPIO0	SF2_D1	CLK	MISO/MOSI	SIG0/SIG4	SCL	PWM_CH0		FEM0	TMS/TCK
7	GPIO1	SF2_D2	CMD	MOSI/MISO	SIG1/SIG5	SDA	PWM_CH1		FEM1	TDI/TDO
10	GPIO2	SF2_D3	DAT0	SS	SIG2/SIG6	SCL	PWM_CH2		FEM2	TCK/TMS
14	GPIO3		DAT1	SCLK	SIG3/SIG7	SDA	PWM_CH3		FEM3	TDO/TDI
11	GPIO4		DAT2	MISO/MOSI	SIG4/SIG0	SCL	PWM_CH4	ADC_CH1	FEM0	TMS/TCK
12	GPIO5		DAT3	MOSI/MISO	SIG5/SIG1	SDA	PWM_CH0	ADC_CH4	FEM1	TDI/TDO
15	GPIO7			SCLK	SIG7/SIG3	SDA	PWM_CH2		FEM3	TDO/TDI
17	GPIO8			MISO/MOSI	SIG0/SIG4	SCL	PWM_CH3		FEM0	TMS/TCK
2	GPIO11			SCLK	SIG3/SIG7	SDA	PWM_CH1	ADC_CH10 /IRTX	FEM3	TDO/TDI
5	GPIO12			MISO/MOSI	SIG4/SIG0	SCL	PWM_CH2	ADC_CH0	FEM0	TMS/TCK
6	GPIO14			SS	SIG6/SIG2	SCL	PWM_CH4	ADC_CH2 /DAC_B	FEM2	TCK/TMS
16	GPIO16			MISO/MOSI	SIG0/SIG4	SCL	PWM_CH1		FEM0	TMS/TCK
4	GPIO20	SF1_D0 /SF2_D0		MISO/MOSI	SIG4/SIG0	SCL	PWM_CH0		FEM0	TMS/TCK

6. Electrical Specifications

6.1 Power Supply DC Characteristics

The digital IO supports VDD33 or VDD18 application.

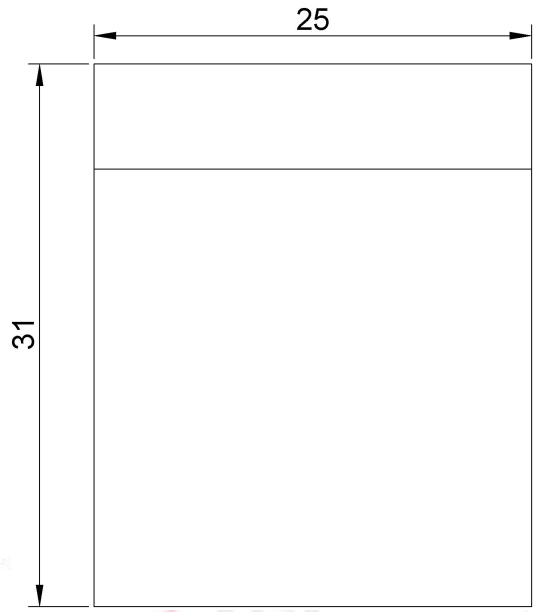
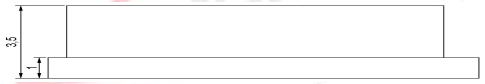
	MIN	TYP	MAX	Unit
Operating Temperature	-20	25	85	deg.C
VBAT	2.1	3.3	3.63	V
VDDIO	2.1/1.62	3.3/1.8	3.63/1.98	V

6.2 Power Consumption

Mode		Note	Performance @3.3Vdc 25°C			
			Min.	Typ	Max.	Unit
RX	11b			35		mA
	11g			39		
	11n			39		
	BLE 1Mbps	Duty 60%		31		
TX	11b - 11Mbps @21dBm	Duty 50%		190		
		Duty 99%		310		
	11g - 54Mbps @18dBm	Duty 50%		145		
		Duty 99%		230		
	11n - MCS7 @17dBm	Duty 50%		130		
		Duty 99%		215		
	BLE 1Mbps @15dBm	Duty 86%		133		

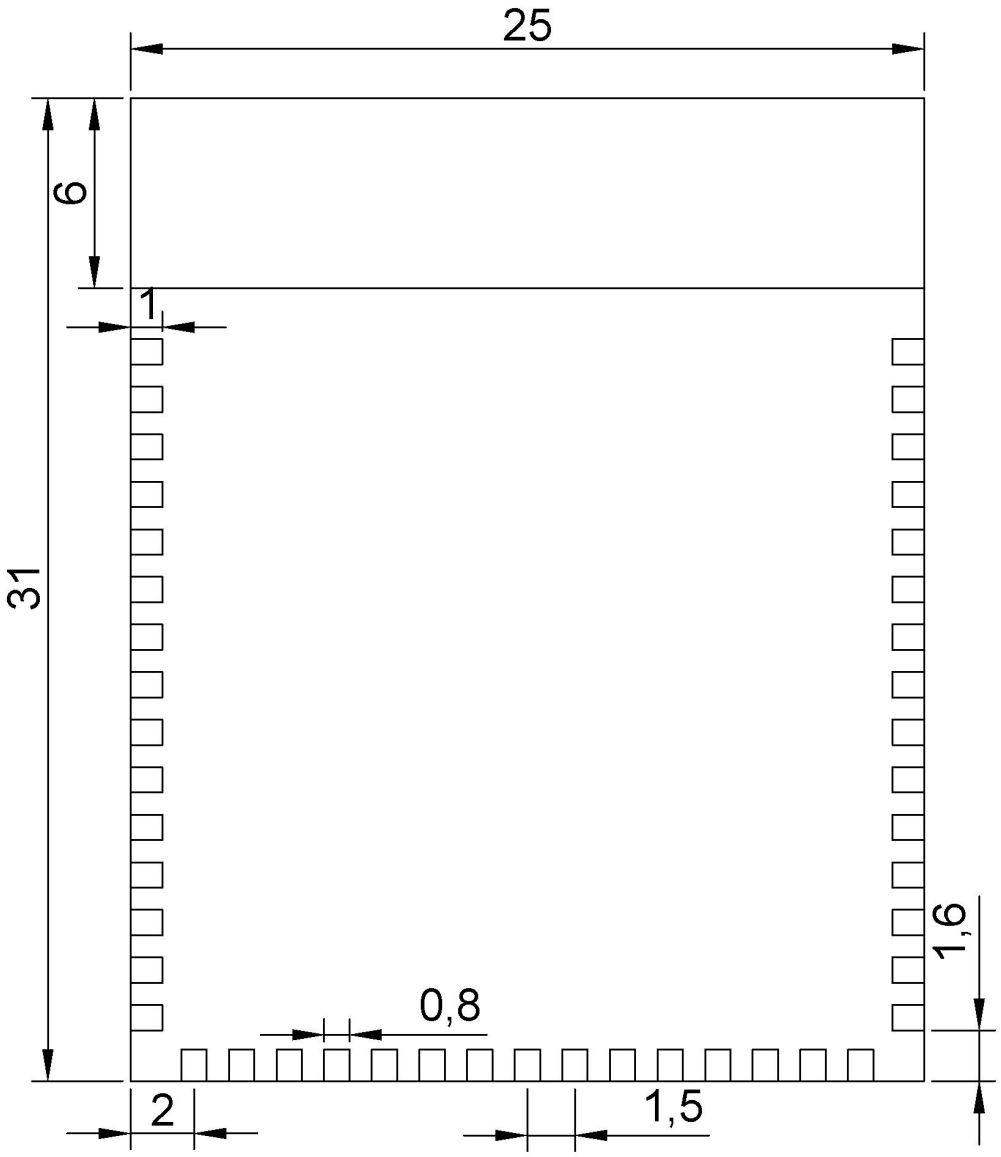
7. Size reference

7.1 Module Picture

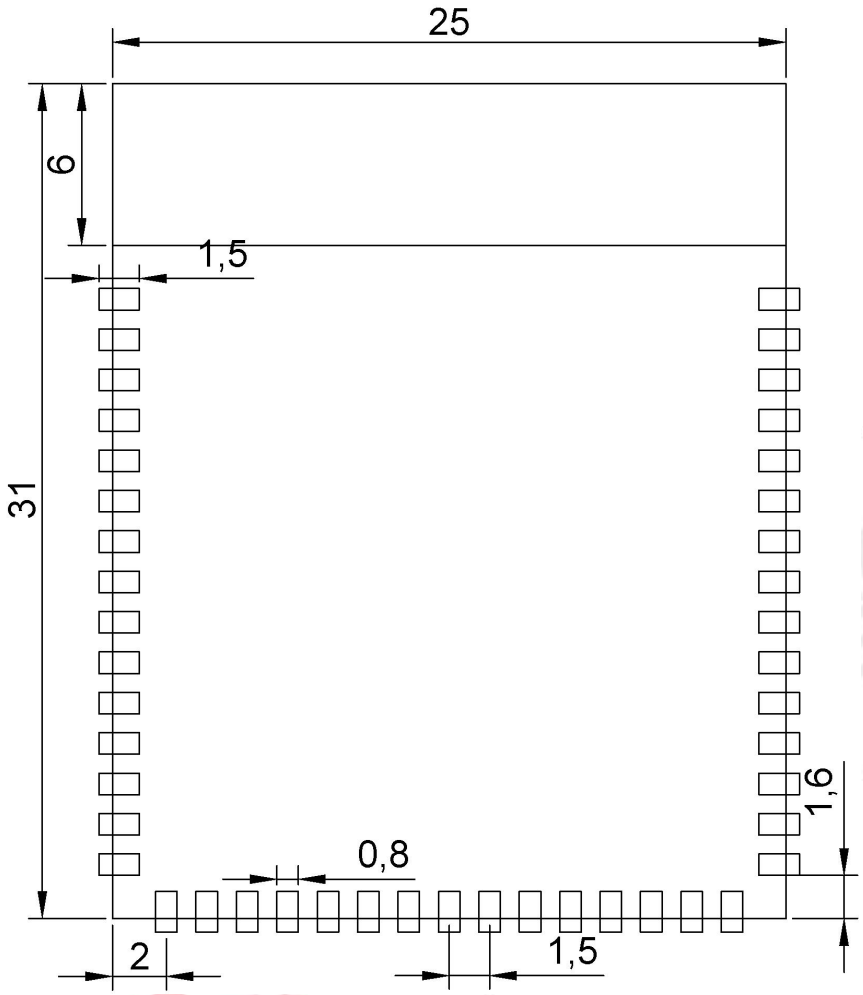
L x W : 31 x 25 (±0.25) mm	
H: 3.5 (±0.2) mm	
Weight	TBD

7.2 Physical Dimensions

<TOP View>



7.3 Layout Recommendation

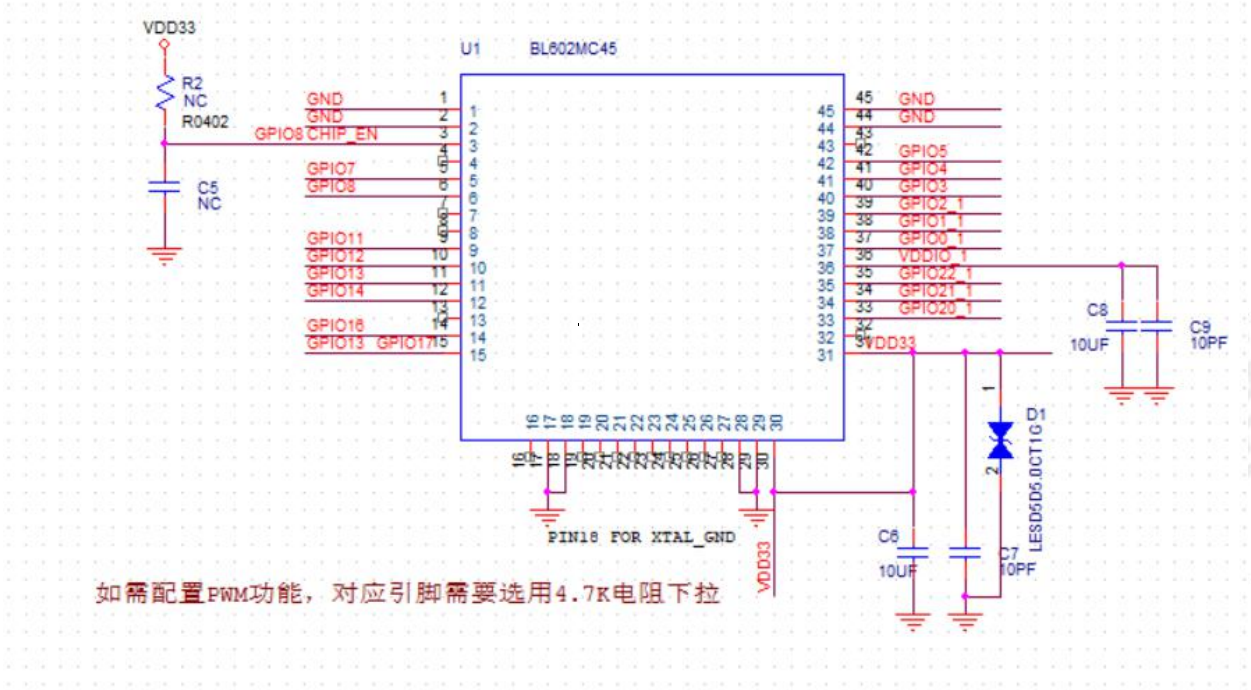


8. The Key Material List

Chipset	BL602C-20-Q2	Bouffalo Lab
PCB	FR4, 4 LAYER, GREEN	XY-PCB, GDKX, Sunlord, SLPCB
Crystal	3225 40MHz ±10ppm	ECEC, Hosonic, TKD, JWT
Inductor	0806 2.2uH,±20%	Murata,sunlord,cenke
Shielding	J102L-R-V1.0	信太，Jlitong

9. Reference Design

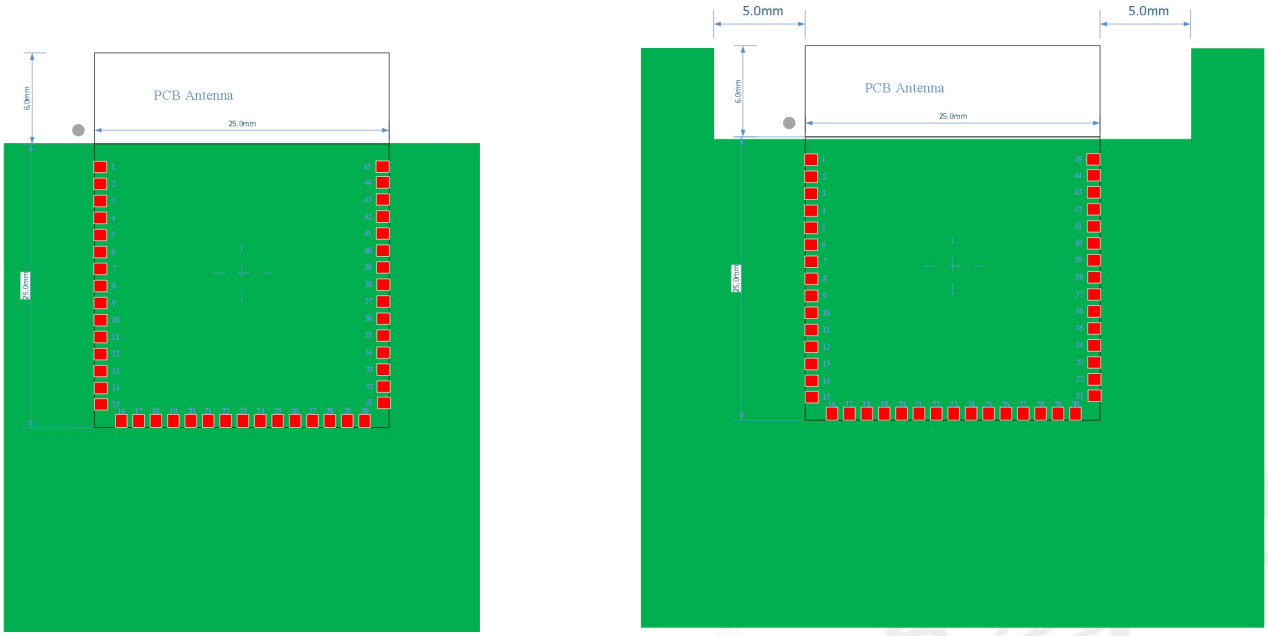
9.1 Reference Design figure



Note: in PWM light control applications,the IO that generates PWM needs to be kept in a definite state during the power-on process(generally is vil),to avoid for flickering condition.

1. during or after power-on, GPIO0~2、5、7、14、20~22 will have vih caused by weak pull-up, can be pull-down by increasing the 4.7K resistance,keep Vil.
2. The default function of GPIO11 is JTAG TDO,VOH may be during power-on,it is not recommended to use is as a pwm light control.
3. other GPIOs are used as pwm light control,lt is also recommended to add 4.7K resistance pull-down ,avoid floating status.
4. when bootstrap gpio8 is Vih ,the default is PROGRAMMER UART when powered on,

9.2 Antenna clearance area requirements



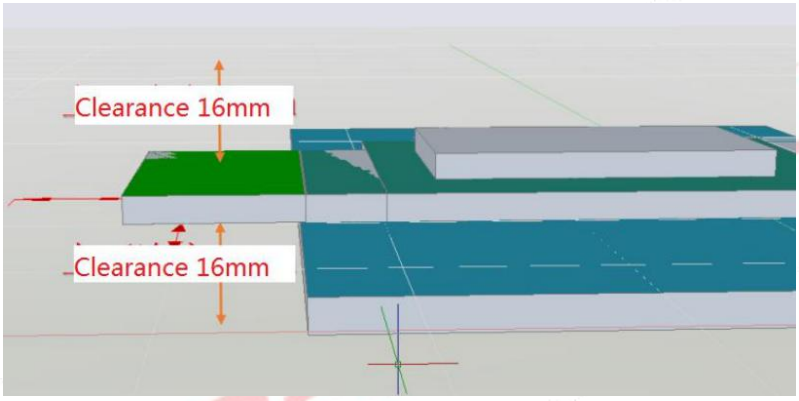


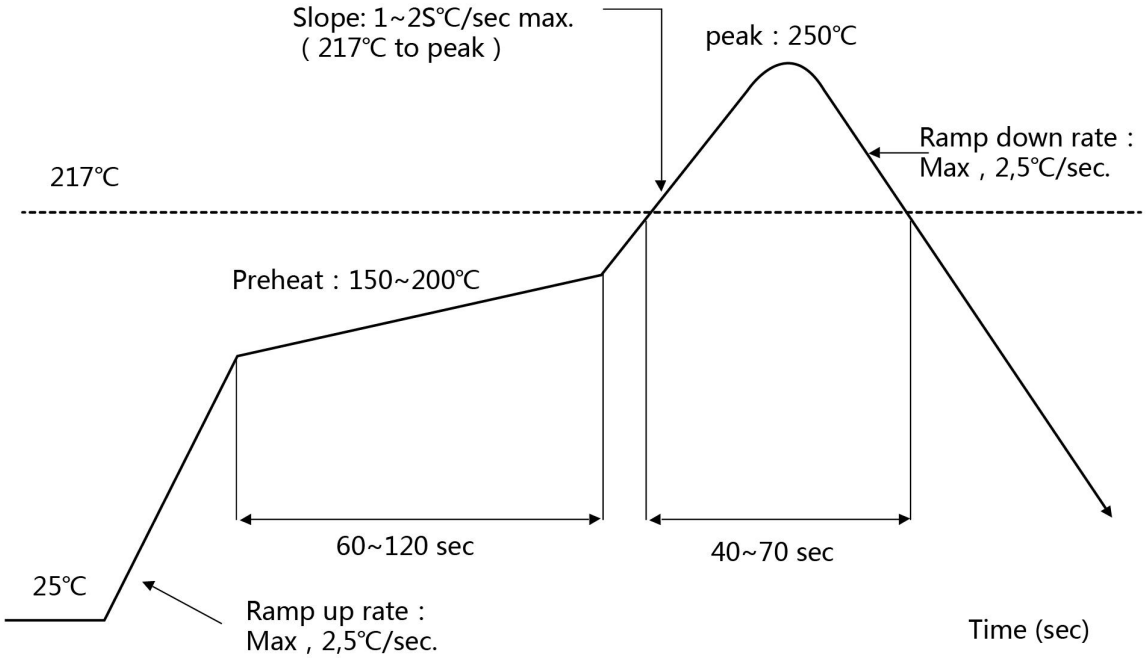
Figure 7-1 antenna clearance area requirements

10. Recommended Reflow Profile

Referred to IPC/JEDEC standard.

Peak Temperature : <250°C

Number of Times : ≤2 times



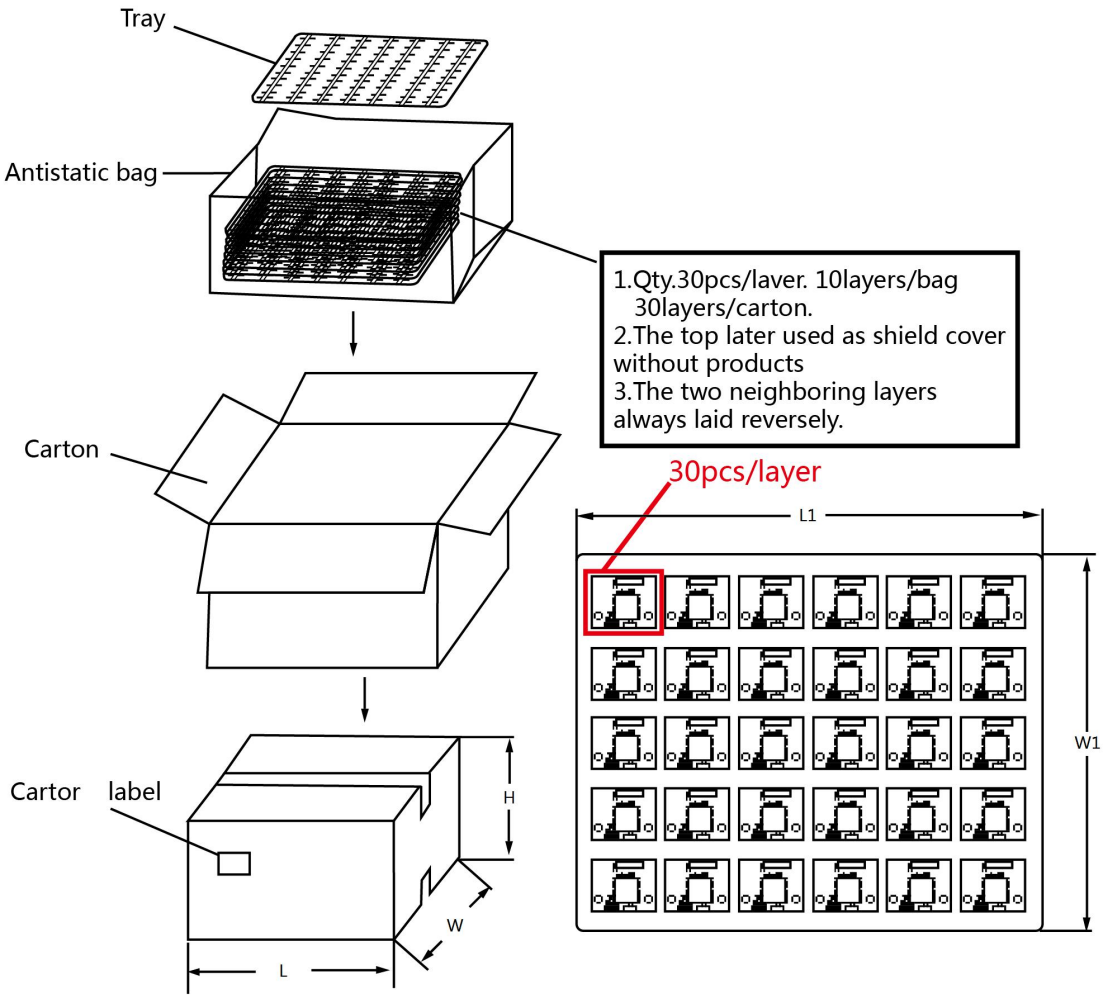
11. Package

Layer size: L1=250mm, W1=190mm

Layer material: PVC

Carton size: L=***mm, W=***mm, H=***mm

Carton material: A=A



12. Moisture sensitivity

The Modules is a Moisture Sensitive Device level 3, in according with standard IPC/JEDEC J-STD-020, take care
all the relatives requirements for using this kind of components.
Moreover, the customer has to take care of the following conditions:

a) Calculated shelf life in sealed bag: 12 months at <40°C and <90% relative humidity (RH)

b) Environmental condition during the production: 30°C / 60% RH according to IPC/JEDEC J-STD-033A paragraph 5

c) The maximum time between the opening of the sealed bag and the reflow process must be 168 hours if condition

b) "IPC/JEDEC J-STD-033A paragraph 5.2" is respected

d) Baking is required if conditions b) or c) are not respected

e) Baking is required if the humidity indicator inside the bag indicates 10% RH or more